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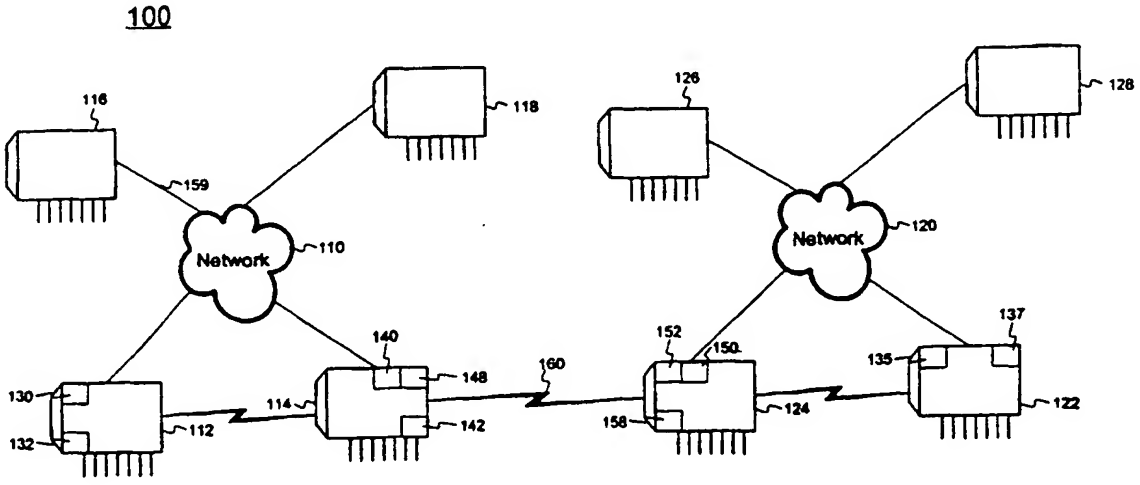

(57) Abstract

A system for transmitting asynchronous transfer mode voice, video, data, and imagery over deployable line-of-sight channels. The system includes an ATM adaptation layer and an ATM cell configuration, which include a flexible multirate encoder and decoder. The ATM cell configuration also entails separate encoding and decoding of header and payload codes, interleaving the header and payload bits, and a methodology for cell synchronization. Using this system, a deployable line-of-sight channel is available for ATM transmissions in a military or tactical environment. Additionally, the system also enables a civilian or commercial ATM channel to operate with a military or tactical ATM channel.

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Description

Method and Apparatus for Transmitting ATM Over Deployable Line-of-Sight Channels

Technical Field

The present invention relates generally to asynchronous transfer mode (ATM) transmissions. More particularly, the invention relates to a method and apparatus for transmitting ATM voice, video, data, and imagery over deployable line-of-sight (LOS) channels.

Background Art

The communication links for the transmission of voice, video, data, and imagery are fundamental building blocks for both commercial and military networks. ATM has efficient bandwidth utilization characteristics, enables simultaneous support for voice, video, data, and imagery, provides inherent support for variable transmission rates, and is commercially available. For these reasons, the use of ATM over different types of communication links is increasing. LOS ATM links and satellite ATM links serve to augment the wired ATM links (*e.g.*, optical fiber links) of the commercial infrastructure networks. The ATM LOS and ATM satellite communications links also often serve as the backbone links for tactical military communications networks, which must be deployed rapidly in the field under a variety of geographical conditions.

In the commercial environment, LOS and satellite links are carefully planned and managed. The deployment of these links in any geographical region requires attention to that region's terrain and atmospheric effects. For example, signal attenuation due to a region's average rainfall can be considered so that sufficient link margin (*i.e.*, sufficient transmitted power and sufficient antenna size) is available to mitigate the attenuation and to provide low bit error rates (BERs), which in turn provide good link quality, for 99.9% of the year on average. Accordingly, when the circumstances allow for such careful planning, it is possible to provide very high quality links (*i.e.*, low BER links). As a result, ATM can be effectively

carried over these links without the need for any additional physical layer error control beyond what is typically used. For example, commercial ATM error detection and correction need not be very robust, because it uses transmission links with BERs of 10^{-9} to 10^{-12}.

In the military environment, however, the demands on communication links are somewhat more strenuous. Moreover, a transition is currently occurring from the traditional time division multiplexed (TDM) based networks to an all ATM infrastructure within the strategic and tactical networks of the United States military, NATO, and other similar organizations. Therefore, for these military and similar applications, it is necessary to provide a physical layer error-control mechanism to combat the challenges presented by certain wireless links. Such an error-control mechanism would enable high-quality ATM networks to be deployed in any situation, regardless of the terrain or atmospheric conditions. After all, in these cases, the circumstances to carefully study the terrain and operating environment prior to installing a wireless link do not exist. For this reason, any such physical layer (PHY) error-control mechanism must provide sufficiently low decoded BER to allow effective ATM transmission even for channel BERs as high as 10^{-3} for data and 10^{-2} for voice.

In order to meet the needs for communication links in the military environment, deployable LOS links (or channels) are ideally suited to provide link service in such extreme situations. Further, deployable LOS channels can also be used as permanent extensions of the infrastructure network or to provide remote access to or from areas where wire line or heavily engineered wireless channels would be prohibitive. These channels can also offer the host of applications which are available over ATM, providing a quick and easily deployable wireless transmission system which is significantly less costly to field and maintain when compared to the alternatives. Yet, along with the obvious advantages of deployable LOS channels, there are inherent limitations. Most notably, commercial deployable LOS channels are subject to bandwidth restrictions and bit error rates (BERs) associated with this type of media. Also, military (or tactical) LOS channels provide BERs of only 10^{-3} to 10^{-6}, thereby compelling more powerful error correction and detection than provided by commercial ATM over standard LOS channels.

Despite these issues, thousands of deployable LOS channels have been successfully used worldwide for more than twenty years. The military constitutes one of the heaviest users of this technology, particularly ground mobile forces. Yet, other examples of users abound, including not only commercial but also civilian government as well as emergency and disaster relief entities. For instance, after the devastating hurricanes that hit Hawaii and Florida in recent years, deployable LOS channels were immediately set-up providing emergency voice and data communication linking together the many islands of Hawaii and servicing those areas in Florida affected by the disaster.

As the use of deployable LOS channels becomes more prevalent for ATM transmissions, however, the combination of civilian and commercial ATM with military and tactical ATM becomes more important. At present, error control sufficient for military/tactical uses requires greater error-correction capability and therefore more overhead than the standard civilian and commercial ATM. Connecting a deployable channel to an ATM link also raises other concerns, such as maximizing transmission efficiency and packaging the types of data seen in deployable LOS (*e.g.*, tactical) environments. As a result, the standard ATM format used by civilian and commercial entities cannot be transmitted reliably over tactical transmission channels.

Disclosure of the Invention

Accordingly, the present invention is directed to methods and apparatuses that permit the connection of ATM networks in tactical environments. Such systems and methods use (1) a new ATM cell configuration; (2) separate encoding and decoding of header and payload codes; (3) a flexible multirate encoder and decoder; (4) interleaving header and payload bits; (5) a new method of cell synchronization; and (6) a unique tactical ATM adaptation layer.

A method consistent with this invention of creating a frame containing tactical payload data comprises the steps, executed by a data processor, of placing a portion of the payload data into a fixed size tactical payload portion of a cell in the frame; forming a tactical fixed size header portion of the cell containing routing information for the cell; and appending a synchronization character to the cell.

A method consistent with this invention of creating a tactical ATM frame from an ATM cell having header data with error detecting/correcting codes and payload data, comprises the steps, executed by a data processor, of placing into a header portion of the frame the header data from the ATM cell other than the error detecting/correcting codes; placing a portion of the payload data from the ATM cell into the header portion of the frame; placing the remainder of payload data into a payload portion of the frame; and appending a synchronization character to the cell.

A method consistent with this invention of creating a frame containing tactical payload data comprises the steps, executed by a data processor, of placing a portion of the payload data into a fixed size tactical portion of a cell in the frame; forming a tactical fixed size header portion of the cell containing routing information for the cell; and encoding the header portion of the cell separately from the payload portion using a first error detecting/correcting code.

A method consistent with this invention of flexibly encoding a portion of a tactical cell for transmission on a channel, comprising the steps of selecting an error detection/correction code to match transmission characteristics of the channel; setting an encoder to implement the error detection/correction code on the portion of the cell by storing generator polynomial coefficients representing the selected error detection/correction code, and shifting in information bits of the tactical cell portion; and forming combinations of the information bits based on the coefficients to encode the tactical cell portion with the selected error detection/correction code.

A method consistent with this invention for transmitting a frame containing tactical payload data bits and header bits comprises the steps, executed by a data processor, of interleaving the header bits and the payload bits by inserting a header bit after a first number of payload bits; and transmitting the interleaved header bits and payload bits.

A method consistent with this invention of creating a frame containing tactical payload data comprises the steps, executed by a data processor, of placing a portion of the payload data into a fixed size tactical payload portion of a cell in the frame; forming a

tactical fixed size header portion of the cell containing routing information for the cell: and appending a synchronization character to the cell that takes alternating values.

A method consistent with this invention of converting a high layer transmission into a format compatible with a tactical cell comprising the steps, executed by a data processor, of multiplexing the transmission into tactical payload data; forming a header for use when reassembling information for the transmission; placing a portion of the payload data into a fixed size tactical payload portion of a cell; forming a tactical fixed size header portion for the cell containing routing information; and setting a synchronization character to the cell.

Both the foregoing summary and the following detailed description provide examples and explanations to persons skilled in the relevant art. These examples and descriptions illustrate, but do not restrict, the claimed invention.

Brief Description of the Drawings

The accompanying drawings, which are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and, together with the description, explain the principles of the invention.

In the drawings:

Figure 1 is a block diagram of a transmission network consistent with this invention;

Figure 2A is a diagram of a standard ATM cell;

Figure 2B is a diagram of tactical ATM frame consistent with this invention;

Figure 3 is a diagram showing an implementation of a tactical ATM cell encoder consistent with this invention;

Figure 4 is a block diagram of a tactical ATM cell decoder consistent with this invention;

Figure 5A shows a system 500 with several encoder/decoder sets for different error detecting/correcting codes;

Figure 5B is a diagram showing an architecture consistent with this invention for providing selectable error coding;

Figure 5C is a diagram showing an architecture consistent with this invention for computing a partial syndrome of a header portion of a tactical ATM frame;

Figure 6 is a block diagram of a flexible decoder consistent with this invention;

Figure 7 is a schematic illustration showing how the standard AAL fits within the ATM protocol stack consistent with this invention;

Figure 8 shows a symbolic view of a generic AAL structure; and

Figure 9 shows a diagram of a TAAL-1 cell consistent with this invention.

Best Mode for Carrying Out the Invention

Systems consistent with the present invention will be described below in accordance with the following table of contents of features included in such systems:

A. Overview

In the following description, the same reference numbers refer to the same or similar elements. The description is organized to show the following six features: (1) a new ATM cell configuration; (2) separate encoding and decoding of header and payload codes; (3) a flexible multirate encoder and decoder; (4) interleaving header and payload bits; (5) a new method of cell synchronization; and (6) a unique tactical ATM adaptation layer. Not every feature need be present in all embodiments of this invention.

Implementing error-control consistent with this invention involves developing a new cell format for transferring standard ATM header and payload data. The new configuration expands the header and permits required error detection and correction. In addition, the header and payload portions of the cell can be separately encoded, such as by specifically chosen binary Bose-Chaudhuri-Hocquenghem (BCH) codes. The code for the header is more powerful than the one for the payload because the header is more important, especially for voice and video transmission. Those transmissions tend to be in real time and require highly reliable delivery of the cell header. Voice and video can tolerate payload errors because those errors only degrade the sound or view temporarily and usually not beyond recognition. Data transmission does not suffer the same problems as video or voice because data transmission typically uses a transport layer automatic-repeat-request (ARQ) scheme that retransmits lost cells or payloads with uncorrectable errors.

Systems and methods consistent with this invention can provide several options to accommodate different payloads. For example, such systems and methods can allow encoding both the header and the payload or just the header. Other systems and methods consistent with this invention can match the error detecting/correcting code to prevailing channel conditions.

In addition, to mitigate the effect of burst errors on the header portion, header bits can be interleaved over the entire cell. Interleaving also breaks up the cyclic structure of the header code, which in turn reduces the probability of decoding the header code incorrectly when a received frame is misregistered. This makes frame synchronization more effective because the frame sync decision is based in part on successful decoding of the header.

Figure 1 is a block diagram of a transmission network 100 that demonstrates where systems and methods consistent with this invention would operate. Transmission network 100 includes network 110, connected to access/switching units 112, 114, 116, and 118, and network 120, connected to access/switching units 122, 124, 126, and 128.

Access/switching units 116, 118, 126, and 128 include commercial ATM units. Accordingly, access/switching units 116, 118, 126, and 128 utilize standard commercial ATM cells in transmissions via networks 110, 120.

Access/switching units 112, 122 include TAAL (tactical ATM adaptation layer) processors 130, 135, respectively, connected to a CVSD (continuously variable slope delta) analog/digital and digital/analog converters 132, 137.

Access/switching unit 114 includes an ATM interface 140, a tactical ATM encoder 142, and a tactical ATM decoder 148. Access/switching unit 124 includes an ATM interface 150, a tactical ATM encoder 152, and a tactical ATM decoder 158.

ATM interfaces 140, 150 follow the necessary protocols for transmitting and receiving standard ATM cells via networks 110 and 120, respectively.

Encoder 142, 152 take the headers and payloads from the standard ATM cells and format them for the tactical ATM cell described below. Figure 2A is a diagram of a standard 53-byte (424-bit) ATM cell 180. The first five bytes form header portion 185, one cyclical redundancy check (CRC) byte 190 addresses error correction, and the remaining 48 bytes (384 bits) comprise payload 195.

Decoders 148,158 take the headers and payloads for the tactical ATM cells and perform the operations necessary to extract the header and payload data for a standard ATM cell. Figure 2A does not show a synchronization character or scheme for the standard ATM cell, but some sort of synchronization approach (*e.g.*, SONET) would be required.

Access/switching units 112, 114, 116, 118, 122, 124, 126, and 128 all communicate with each other over a commercial wired link 159.

Access/switching units 112, 114, 122 and 124 also communicate with each other over a deployable LOS channel 160. Access/switching units 114, 124 repackage ATM data for transmission over channel 160. Encoders 142, 152 convert data, usually in the form of a standard ATM cell, into a format of a tactical ATM cell. The data for the tactical ATM cell, however, need not come from a standard ATM cell, nor need the data from the tactical cell be placed into an ATM cell, although Figure 1 shows such a connection.

Deployable LOS channel 160 preferably comprises a tactical channel, more specifically a tactical LOS channel, but channel 160 may also comprise a satellite channel or any other form of deployable LOS channel. The implementation utilized by the preferred embodiment was developed primarily for the tactical LOS channels used by the U.S. Army.

For these channels, (noncoherent) binary frequent shift keying (FSK) is used as the modulation format for the implementation of binary hard decisions. These channels generally experience BERs from 10^{-3} to 10^{-6} with Rician fading. Also, for design and analysis purposes the U.S. Army uses a burst-error specification (Section 3.2.1.1.1.2.1.9 of "Performance Specification Central Office Telephone, Automatic AN/TTC-39 () (V)," Specification No. TT-B1-1101-0001C, Joint Tactical Command, Control and Communications Agency, Fort Monmouth, New Jersey, June 15, 1984).

A satellite channel is less severe than the tactical LOS channel, because it does not experience fading and generally has BERs on the order of 10^{-6}. However, the satellite channel typically uses quadrature phase-shift-keying (QPSK) or binary phase-shift-keying (BPSK) modulation formats usually combined with convolutional coding. Because the satellite channel is less severe than the tactical LOS channel, the disclosed implementation can be readily used over a satellite channel. Indeed, the disclosed implementation would result in even better performance over satellite channels than over LOS channels.

Further, in the preferred implementation, the deployable LOS channel may embody a stand-alone unit or, alternatively, may embody a converter unit, allowing a commercial channel to function as a deployable tactical LOS channel. In this alternative implementation, the converter unit would allow both commercial and tactical uses as a communication channel. For example, the preferred embodiment is designed primarily for use over tactical channels, particularly line-of-sight (LOS) channels, which experience Rician fading. The BERs associated with these LOS channels range from 10^{-3} to 10^{-6}. However, the disclosed invention would be useful and beneficial for transmission of ATM over any channels where the BER is higher than the typical commercial BERs of 10^{-9} to 10^{-12}. Therefore, for simplicity, the disclosure uses the terms "tactical ATM," "tactical header," "tactical payload," etc. to refer to the preferred embodiment. However, the use of this terminology does not preclude use of the invention in non-tactical commercial applications where the channel quality is poor (*i.e.*, where the channel BER is high).

1. ATM Cell Configuration

Figure 2B is a diagram of tactical ATM frame 200 consistent with this invention. In the system shown in Figure 1, encoders 142, 152 would build frame 200, and decoders 148, 158 would extract data from frame 200.

Frame 200 includes a 5-bit synchronization character 210 and a 503-bit Tactical ATM cell 220 containing header and payload information from a standard ATM cell. The total frame (synchronization character plus tactical ATM cell) consists of 508 bits, for a transmission efficiency (payload per cell) of 384 payload bits/508 total bits, or 75.6%. The transmission efficiency of a standard ATM cell is 48/53, or 90.6%.

Tactical ATM cell 220 includes a header 230 and a payload 240. Header 230 contains five bytes (or 40 bits) of data and 42 header parity check bits 235 consistent with an (82, 40) BCH header code that can correct up to six errors in the header portion. If the tactical ATM cell was formed from a standard ATM cell, the forty bits from header 230 would preferably include the thirty-two bits from the header portion of the standard ATM cell, excluding the CRC byte, and the first eight bits from the payload portion. The eight CRC bits are discarded because header position check bits 235 serve the same or similar function, using the (82, 40) header code.

Payload 240 of tactical ATM cell 200 contains 376 bits from the payload portion of the standard ATM cell (384 payload bits less the eight bits placed in header 230) plus 45 payload parity check bits 245. This (421, 376) BCH payload code can correct up to five errors in the payload. Notably, the natural block length of a primitive BCH code is defined as $n=2^m-1$, where m is an integer. The code corrects all error patterns up to t errors, so the minimum distance between codewords is 2t+1. Therefore, at least t+1 bit errors must occur before one codeword can be decoded into a different codeword. The codeword contains $n-k=r \leq mt$ parity check bits. An unshortened codeword has k information bits, where k=n-r.

The placement of the eight payload bits into the header provides a special benefit when payload 240 contains voice data. In that case, the first eight bits of the payload portion constitute an ATM adaptation layer - Type 1 (AAL-1) header. Although not part of the ATM cell header, AAL-1 header is critical to the processing (*i.e.*, reassembly) of the voice payload.

Indeed, the more powerful (82, 40) header code, rather than the (421, 376) payload code, protects the first eight tactical AAL-1 header bits for voice transmission.

As Figure 2B shows, the 40 bits of tactical ATM cell header 230 include (1) a three-bit field 252 for a virtual path identifier (VPI) or for link maintenance (LM) information, (2) a nine-bit field 250 for VPI, (3) a sixteen-bit field 254 for a virtual channel identifier (VCI), (4) a three-bit field 256 for a payload type indicator (PTI), (5) a one-bit field 258 for cell loss priority (CLP), and (6) an eight-bit field 260 representing either the first eight payload bits or the AAL-1 header, as explained previously.

2. Separate Encoding of the Header and Payload

a. Header-only Encoding

One way to increase transmission efficiency is to encode and decode just the header, and leave the payload alone. The header and the first eight payload bits would still use the (82, 40) code, and the header structure would remain the same. The remaining 376 payload bits, however, would remain uncoded, and five-bit synchronization character 210 would still precede header 230. The resulting header-only encoded frame contains 463 bits, raising the transmission efficiency to 384/463 or 82.9%.

b. Error-control Codes

The (82, 40) and (421, 376) error detecting/correcting codes are binary BCH codes. These codes are very powerful. For a random (*i.e.*, independent) error channel operating at a BER of 10^{-5}, the (421, 376) BCH code provides a BER for the payload equivalent to commercial quality links (BER < 10^{-10}). For a random error channel operating at a BER of 10^{-3}, the (421, 376) code provides a decoded BER performance for the payload equivalent to a BER < 10^{-7}. These payload BERs are sufficiently low such that TCP/IP requires few retransmissions for packet sizes of interest, thereby resulting in generally high throughput efficiency.

For a random error channel operating at a BER of 10^{-3}, the (82, 40) header code provides a cell loss ratio (CLR) of 3.6×10^{-12}. For a tactical LOS link operating at an average BER of 10^{-5}, the (82, 40) header code provides a cell loss ratio (CLR) of 2.7×10^{-18}. The low

CLRs are essential for voice transmission, because, as explained above, voice transmission will be acceptable at these tactical LOS link BERs as long as the cell is reliably delivered.

One advantage of these codes is their performance over Rician fading channels. The Rician fading channel provides a reasonable model for the LOS channel and is more severe than the random error channel. For K = 10 dB and K = 20 dB Rician channels at average BERs of 10^{-3} and 10^{-5}, the cell loss ratio and the decoded BER performance for the payload are low enough to support voice, video, data, and imagery transmission.

The header code (82,40) and the payload code (421, 376) represent a baseline. Other block codes may be used depending on the channel conditions and the desired level of error-control. And, consequently, the use of other codes could increase or decrease the tactical frame size.

3. Hardware Design

a. Tactical ATM Cell Encoder

Figure 3 is a diagram showing an implementation of a tactical ATM cell encoder 300 consistent with this invention. Encoder 300, which could serve as encoders 142 and 152 in Figure 1, receives cells having the standard ATM cell format. Preferably, encoder 300 is implemented in a single Field Programmable Gate Array designed using VHDL (VHSIC Hardware Description Language). Of course, many other implementations and designs are possible.

In this embodiment, encoder 300 provides four major functions: (1) generate header parity; (2) generate payload parity; (3) interleave header; and (4) cell framing. The preferred implementation of encoder 300 has separate elements to perform these functions, although the same element can perform combinations of the functions as well.

Header parity generator 310 extracts the first four bytes of the ATM cell header and the first byte of the cell payload and processes them according to the (82,40) BCH code to create a codeword with 40 information bits and 42 check bits. Header parity generator 310 uses a linear-feedback, 42-bit shift register for the processing, although other circuitry, such as a microprocessor, could also be used.

Payload parity generator 320 processes forty-seven payload bytes (all but the first payload byte) using a (421, 376) BCH code to create a codeword with 376 information bits and 45 check bits. Payload parity generator 320 preferably includes a 45-bit linear feedback shift register.

Control 330 causes multiplexer 340 to interleave the 82 header codeword bits across the 421 bits of the payload codeword (or 376 bits if not using payload encoding/decoding). As explained below, one method of interleaving has every fifth bit as a bit from the header codeword, starting with the first bit.

Control 330 also causes multiplexer 340 to insert the five bit synchronization character from sync character generator 350 at the beginning of each cell. The complete encoded ATM cell includes 508 bits as shown in Figure 2B (assuming that both header encoding and payload encoding are used).

Parallel-to-serial register 360 converts the encoded signal into a serial, BCH-encoded ATM cell bitstream 370 with the appropriate clock 380. This is the cell sent over tactical channel 160 (Figure 1).

b. Tactical ATM Cell Decoder

Figure 4 is a block diagram of a tactical ATM cell decoder 400 that receives a 508-bit serial bit stream over tactical channel 160 (Figure 1). Decoder 400 provides four major functions: (1) detect framing characters; (2) determine header and payload syndrome; (3) apply the Massey algorithm; and (4) perform Chien search/error correction.

Decoder 400 includes a frame processor 410 that uses correlation to detect the frame characters. Frame processor 410 examines the incoming bit stream and searches for the five-bit sync characters that precede each ATM cell. As explained below, processor 410 verifies framing by ensuring correct decoding of the ATM cell header.

Separate header and payload syndrome processors 420, 425 independently analyze the header and payload bits. In the preferred implementation, header and payload syndrome processors 420, 425 use six-bit and five-bit linear feedback shift registers, respectively. RAM 430 stores the header and payload bits from processors 420, 425 until digital signal processor 440 completes the Massey algorithm.

The receipt of an entire cell by processors 420, 425 generates an interrupt to digital signal processor 440, which implements a Massey algorithm, a known algorithm for decoding BCH-encoded data. The Massey algorithm produces up to six error locator polynomial coefficients for a header codeword and up to five error locator polynomial coefficients for a payload codeword. Details about the Massey algorithm appear in J.L. Massey, "Shift-Register Synthesis and BCH Decoding," IEEE Transactions on Information Theory, IT-15 pp. 122-127 (1969).

Chien search function processor 450 retrieves the stored ATM cell from dual port RAM and corrects the header and payload bits using those error locator polynomial coefficients. Preferably, Chien search function processor 450 has six and five linear feedback shift registers for the header and payload, respectively. Details about the Chien search function appear in R.T. Chien, "Cyclic Decoding Procedures for Bose-Chaudhuri-Hocquenghem Codes," IEEE Transactions on Information Theory, IT-18, pp. 357-363 (1964).

The number of bits corrected should equal the degree of the error locator polynomial. Disagreement indicates uncorrectable bit errors. If an uncorrectable error occurs in the cell header, processor 450 discards both the header and payload. If an uncorrectable error occurs in the cell payload, processor 450, at its own discretion, passes the payload along unaltered. As explained above, errors in voice and video are acceptable, and the TCP/IP functions will handle payload errors by requesting retransmission. Counters in processor 450 record the total number of received cells, the number of cells discarded due to decoding failure of the header code, and the number of bits corrected for later link performance analysis and to support the flexible rate design.

Tactical ATM cell decoder 400 preferably includes both VHDL-coded hardware and assembly language firmware. Frame processor 410, header and payload syndrome processors 420, 425, and Chien search function processor 450 are preferably implemented in two field-programmable gate arrays. Digital signal processor 440 is preferably implemented in firmware. Of course, other technologies may also be used.

4. Multirate Encoder/Decoder

Variable channel conditions have forced conventional encoders and decoders to adopt an error correction/detection code set for a worst case condition. Systems and methods consistent with this invention improve the efficiency of the tactical ATM format by selecting error correction/detection codes to match current channel conditions. The code of choice is the highest efficiency code that produces the quality of service required for the current channel BER. This is because the higher the efficiency, the fewer the number of parity bits, and the lower the overhead (code parity bits) when channel conditions are less severe.

Binary BCH codes provide a handy mechanism for such flexibility because the existence of a large number of binary BCH codes provides a wide selection of block length, rate, and error-correction power from which to choose. Furthermore, BCH decoders can be configured to compute the average number of errors corrected per codeword, which provides the information needed to control rate changes. The full-duplex communication circuits for tactical ATM provide a mechanism to request rate changes.

Figure 5A shows a system 500 with several encoder/decoder sets 510-512, where each set implements a different error detecting/correcting code. Each encoder/decoder set is comprised of three key parameters: (1) the number or errors to be corrected; (2) the primitive polynomial coefficients; and (3) the generator polynomial coefficients. The first two parameters are used to configure the hardware. The encoder/decoder sets 510-512 illustrate three parameter sets that could be used to configure a single, double, and triple error detection and correction code for the header. A similar set of parameters would be required to configure the payload error detection and correction code.

Figure 5B is a diagram showing one possible alternative architecture for providing selectable error coding. Flexible encoder 520 configures itself to process codes in the desired range.

Encoder 520 takes advantage of the fact that BCH codes are cyclic codes defined by a generator polynomial g(x) of degree r, where r is the number of parity check bits per codeword. Encoder 520 uses a linear feedback shift register circuit with r stages because it can generate codewords with the desired structure. By modifying the data used to generate

the codewords, the flexible architecture of encoder 520 can implement BCH codes defined by generator polynomials with degrees less than r.

A control 525 in encoder 520 initializes shift register 530 by setting its storage elements 532, 533, 534, 535, and 536 to zero, and loading the generator polynomial coefficients g_i into coefficient register 540. Next, control 525 produces the parity check bits of a codeword by shifting the information bits (ij) into communications channel 550 and the shift register 530 while feedback is enabled. After processing the last information bit, shift register 530 contains the r parity check bits. Clocking register 530 r more times with the feedback disabled shifts the r parity check bits into the channel. This last operation also reinitializes the register storage elements to zero.

Shortening the code by reducing the number of information bits per codeword, while keeping the same number of parity check bits, provides improved error correction performance. Shortening a code by s bits produces a block of length n' = n-s that protects k' = k-s information bits with r parity check bits per codeword. The shortened code may be used to correct the same number of errors as the unshortened code.

A BCH code is shortened by eliminating the s most significant information bit positions. The k' information bits are shifted simultaneously into shift register 530 and the communication channel and the r parity check bits are determined as before. This effectively involves setting the leading s information bit positions of the unshortened code to zero. Because leading zeroes have no impact on the encoding process, they are discarded.

The (82,40) and (421,376) codes are shortened BCH codes to match the payload and header sizes. The (82,40) code is the (127,85) code shortened by 45 bits. The (421,376) code is the (511,466) code shortened by 90 bits.

The architecture of shift register 530 accommodates polynomials with degree $r' < r$. Doing so requires loading the r' coefficients into coefficient register 540, aligning the most significant bit of the polynomial with the most significant bit of register 530. The remaining least significant bit positions of register 530 with no coefficients are set to zero. This effectively masks the unneeded stages of the register without altering the input or output circuitry.

In the preferred implementation, control 525 would determine the appropriate code and control the loading of coefficients and codewords appropriately. Preferably, control 525 would indicate to the decoder the information necessary to decode the flexibly encoded words.

Encoder 520 has r single bit registers that contain all the coefficients g_0 -g_{r-1} of a binary polynomial with coefficients from GF(2) of degree r. The most significant bit g_r is hard-wired to a "1" and provides the feedback from the shift register's most significant bit. If a coefficient is a "1," the AND gate for that coefficient will be enabled, allowing the shift register's MSB to be XORed with the normal input to the corresponding shift register stage. If the coefficient is "0," the feedback is disabled and the normal input will be unmodified.

To use the same circuit to encode data using another generator polynomial g' of degree r'<r, the r' binary coefficients are loaded into the corresponding g_i registers, starting at the highest order. The remaining low order registers are disabled by loading them with a "0."

Figure 5C shows a block diagram of a seven stage generalized shift register. Such a shift register is used by a flexible decoder to compute a partial syndrome of the header portion of the tactical ATM frame. Note that each bit of the shift register, b0 through b6, is interconnected to all shift register bits through a set of seven AND gates followed by an Exclusive-OR tree. The AND gates select which of the shift register bits, b0 through b7, contribute to the feedback at a specific bit position. The feedback is enabled by the mask register values mi,j which are specified by the mask value tables of Figure 5A. For example, if the shift register of Figure 5C is to be configured to compute the S1 partial syndrome for the single error correcting code of Figure 5A, the mask register values, m1,j (j=0, 1, ... 6), are the seven hex numbers listed under the column S1/C1. For example, the mask register value 20(H) = 100000(B) selects feedback from bit position b5 to be summed with the incoming received message bit ri to form the input to b0. The mask register values in the table are generated directly from the primitive polynomial which specifies the code.

Figure 6 is a block diagram of a flexible decoder 600, consistent with this invention, that performs the three steps of decoding a binary BCH codeword: (1) computing the

syndromes of the received word; (2) finding the error locator polynomial from the syndromes; and (3) finding the roots of the error locator polynomial and correcting the errors. Decoder 600 includes syndrome computer section 610, Chien search section 620, and Massey algorithm section 630. Both syndrome computer section 610 and Chien search section 620, the section that finds the roots of the error locator polynomial, can be implemented with generalized feedback shift register circuits. The Massey algorithm is implemented in a general way that allows selection of the maximum number of errors to be corrected.

Decoder 600, capable of correcting t errors in a received codeword, will have either t or 2t generalized shift registers 611, 612, ..., 614 (t shown) for computing the syndromes and an additional t generalized shift registers in the Chien search section 620. If t generalized shift registers are used for the syndrome calculation, the other t syndromes are computed by squaring. Details about syndrome calculation appear in W.W. Peterson, "Error-Correcting Codes," MIT Press, Cambridge, MA, 1961. Each of the generalized shift registers 611 - 614 and 621 - 624 has m stages to operate on codewords up to 2^m -1 bits.

Massey algorithm section 630 includes a programmable processor 631. Preferably, processor 631 and the 2t or 3t generalized shift registers for the syndrome computation and the Chien search are integrated into an application specific integrated circuit (ASIC). The ASIC contains sufficient memory storage locations to hold all necessary shift register configuration data.

Decoder 600 is initialized by providing Massey processor 630 with (1) the number of errors to be corrected, t; (2) the degree, m, of the primitive polynomial p(x) used to obtain the representation of GF(2^m); (3) the m-tuple representing the coefficients of p(x) from GF(2); and (4) the shortened code word length $n' \leq n = 2^m - 1$.

Massey processor 631 will configure itself and generate a table of m-tuples representing GF(2^m). Processor 631 will also write the shift register configuration mask values $M_{k,i+j}$, represented as the matrix M^T, to a configuration memory 632.

This design enables a very high speed integrated circuit (VHSIC) binary BCH decoder that can reconfigure itself as channel conditions vary. The architecture also allows

selection of code rate and error correction power to match channel conditions. Efficiency is improved by selecting the highest rate code that provides the required QOS.

5. Interleaving

Errors usually come from noise or fading in the channel. Independent errors occur randomly, but other correlated errors occur in bursts. Burst errors present special problems because they sometimes overwhelm the error-correcting capability of the code and prevent error correction. Burst errors manifest as a set of consecutive erroneous bits or consecutive bits bounded by erroneous bits with approximately half of the bounded bits being erroneous.

Maintaining low cell loss in the presence of burst errors is important for voice and video transmission because, as explained above, timely cell delivery is particularly important.

Interleaving header 230 with payload 240 mitigates the effect of burst errors on the tactical ATM cell 220 because spreading out the header bits 230 over cell 220 reduces the consecutive nature of any errors. Cell loss with proper interleaving will occur only for very long bursts.

For simplicity, the five sync bits in sync character 210 at the beginning of each tactical ATM frame 200 are not interleaved with the header and payload. Instead, sync character 210 remains at the beginning of each frame. Sync character 210 appears at the beginning of each frame.

The preferred interleaving for frame 200 alternates four payload bits with a header bit to create the following pattern within each frame:

S-S-S-S-S-H-P-P-P-P-H-P-P-P-P-H-P-P-P-P-H-P-P-P-P-H- . . . ,

where S represents a sync bit. H represents a header bit, and P represents a payload bit. This pattern cannot hold for the entire frame because there are 421 payload bits and only 82 header bits. Therefore, only the first 82 sets of four payload bits are interleaved. This leaves 421 - (82 x 4) or (421 - 328) = 93 payload bits to follow the last header bit at the end of the cell. The natural order of the payload bits is otherwise unaltered.

Inserting four payload bits between each header bit works both when the header and the payload are both encoded and when only the header is encoded. In the latter case, there are (376- 328) = 48 payload bits following the last header bit at the end of the cell.

Interleaving also helps during synchronization. Cell or frame synchronization is based on the occurrence of two unrelated events, detection of synchronization characters and successful decoding of a header codeword. The interleaving technique removes the cyclic structure of the header code and reduces the probability of incorrect decoding when the cell is slightly misregistered. This reduces the probability of false framing.

6. Cell Synchronization

Cell synchronization uses the 5-bit framing character 210 at the beginning of each frame 200 (Figure 2B). During acquisition, frame processor 410 generates a tentative framing hypothesis only after successfully detecting two sync characters preceding two consecutive cells. Strictly requiring detection of two characters with no discrepancy (*i.e.*, with no errors) also reduces the probability of false synchronization. The combination of interleaving reducing incorrect decoding probability and requiring detection of the sync characters with no discrepancies results in a false sync probability that is acceptably low.

If, after successfully detecting two consecutive sync characters 210, frame processor 410 then successfully decodes the header codeword following the second sync character, frame processor 410 declares a successful framing. Otherwise, frame processor 410 begins another attempt to detect the framing characters. Once synchronization has been established, if frame processor 410 thereafter fails to decode the header for two consecutive cells, it declares framing to be lost.

The preferred bit sequences for the sync character values are the following five-bit patterns, which alternate: 10001 and 01110. These character values alternate with each successive tactical ATM cell (*e.g.*, 10001, 01110, 10001, 01110, •••••). Therefore, a valid ten-bit framing pattern (from two consecutive cells) will be either a 1000101110 pattern or a 0111010001 pattern.

The 10-bit framing pattern is split into two synchronization fields (*i.e.*, 5-bit characters preceding two consecutive cells) for two reasons. First, doing so halves the

transmission bandwidth overhead of the framing character. Second, splitting the pattern also takes advantage of the repetitive nature of the ATM cell traffic (*e.g.*, idle cells which are all ones).

The tactical ATM idle cell mentioned earlier complies with the ATM Forum/ITU standard. The VPI/VCI fields are all zeroes, except for the LM bits when the link maintenance mode is turned on. The payload of the idle cell is all ones to avoid use of all zeroes that can create confusion with BCH codewords that contain all zeroes. A misregistered word containing nearly all zeroes might be decoded incorrectly, which can lead to false framing.

The framing characters and split framing patterns described above decrease the probability of a false frame hypothesis. One pattern has a string of at least four zeroes, which does not occur in the interleaved idle tactical ATM cell. The string of fewer than four successive ones in the other pattern avoids the dominant four consecutive ones of the interleaved tactical ATM idle cell.

In addition, the two sync fields have five bits that are opposite from their corresponding bits in the other pattern. These "antipodal" bits reduce the probability of a false frame hypothesis, because the sync field of the framing pattern is spread across two consecutive cells. In the case of consecutive identical cells, a false frame hypothesis is impossible, because even if each cell's header and payload would be identical, each cell's sync field would be different. If a match were to occur in one sync field, then by definition, the other sync field, which is different by four bits, would not match because the sync fields are compared against the same bit positions within two consecutive cells.

The mean acquisition time is less than the time required to receive three tactical ATM cells. The probability of false framing is 1.7×10^{-7} per attempt. The probability of falsely declaring loss of framing is 1.3×10^{-23} on a 10^{-3} random error channel. The probability of correctly declaring loss of framing is 0.9998.

With the previous explanations of error detecting/correcting codes, interleaving, and synchronization, the entire cell can be understood. The basic format has the 5-bit framing character (either an A=10001 or a B=01110) followed by 503 bits that represent the header

and payload codewords. The 82-bit header codeword is interleaved within the 421-bit payload codeword using a separation of four between adjacent bits. The header code can correct up to six bit errors in each received word, and interleaving means that for there to be more than six errors in a received word, a solid burst of errors must affect at least thirty-five consecutive channel bits.

The basic cell format is repeated to accommodate transmission of a long sequence of tactical ATM cells. The framing characters alternate so that each transmitted cell is registered by either an AB or a BA pattern. Thus, detection of either framing pattern with the required 503 bit separation defines a framing hypothesis.

To achieve a small false alarm probability, an exact AB or BA match must occur. Once a tentative hypothesis is generated, it is tested by deinterleaving an encoded cell and attempting to decode the resulting header codeword. If the decode attempt is successful, *i.e.*, six or fewer errors are corrected, the framing hypothesis is validated. Otherwise, the search for another hypothesis continues.

The following thus describes the framing algorithm:

(1) Retain incoming bit stream in temporary storage.

(2) Test for occurrence of framing pattern AB (or BA).

(3) Test temporary storage for alternative framing pattern BA (or AB), displaced by 503 bits, with no discrepancies. If not, go to step (5).

(4) Deinterleave the header codeword in the hypothesized cell that follows a detected framing character, and attempt to decode the corresponding header codeword. If that attempt is successful, *i.e.*, if six or fewer errors are found and corrected, declare framing acquired and begin delivery of decoded header and payload data. Otherwise, go to step (5).

(5) Slip the registration assumption and return to step (2).

In this algorithm, one successful header decode is required for validation of a framing hypothesis, and two consecutive header decode failures are required to declare loss of framing. Yet, other parameters could be used for either determination.

7. Tactical ATM Adaptation Layer Type 1

The ATM Adaptation Layer (AAL) adapts higher layer transmission formats into formats compatible with the ATM layer. The AAL type depends on the type of higher layer format transmitted. Voice, video, and data all require different AALs.

In the commercial environment, ATM networks transmit analog voice through the telephone network as 64 kb/s pulse code modulated (PCM) words. Individual 64 kb/s PCM calls (DS-0) are time-division multiplexed into groups of 24 (DS-1). These groups of 24 calls are in turn multiplexed into higher level (multiple of 24) groups. Thus, for commercial ATM, Type 1 AAL (AAL-1) can convert a single 64 kb/s PCM call or a group of N multiplexed 64 kb/s PCM calls into 384 bit segments for insertion into the payload of a standard ATM cell 180 (Figure 2A).

More generally, commercial implementations of AAL1 for PCM voice are typically designed to interface to T1 (24 channel) or E1 (32 channel) groups. These T1 or E1 groups are either encapsulated into cells as a whole (referred to as Unstructured AAL1) or the individual 64 Kbps channels are demultiplexed and are individually, or in groups of N (N=1 to 24 for T1, 1 to 32 for E1) encapsulated into cells (referred to as Structured AAL1). Each channel on the T1 or E1 group operates only at 64 Kbps and can be voice or data. Standard Structured AAL1 multiplexes up to 47 bytes of data into a single cell. Each byte corresponds to a channel on the source T1 or E1 groups, except in some modes where A/B bit signaling information occupies some of the last bytes in the cell. Individual channels can be repeated within a specific cell, and if more than one channel is assigned to a cell stream (AAL process), the repetitive pattern of channels can span many cells. In this case, a Structure Pointer is used so that the receiving end can determine how to reassemble the cell stream and multiplex the channels into the proper time slots on the T1 or E1 interfaces. This eight-bit Structure Pointer takes up an additional byte in the cell payload once every eight cells, leaving only 46 bytes for PCM source channels in that particular cell.

Figure 7 is a schematic illustration showing how the standard AAL fits within the ATM protocol stack consistent with this invention. The AAL for a specific service type

(*e.g.*, data or voice) will convert the user's information into ATM format and then reassemble the user's information into the original format for delivery to the destination.

Figure 8 shows a symbolic view of a generic AAL structure. Essentially, an AAL processor successively encapsulates segments of the user's information stream with headers or trailers until it creates an ATM payload. At the destination node, an AAL processor converts the payload back into the original format using the header and trailer information to indicate to each of the AAL sublayers how to process the incoming encapsulated information.

The standard AAL will not work in the tactical environment, because the tactical environment, A/D and D/A converters, such as CVSD (continuously variable slope delta) analog/digital and digital/analog converters 132, 137 (Figure 1), respectively, convert analog voice into 16 kb/s and 32 kb/s CVSD-modulated signals and vice versa. Instead, systems and methods consistent with this invention require TAAL-1 processors 130, 135 (Figure 1). Those processors package CVSD-modulated signals into payload segments for transmission in tactical ATM cells having the format shown in Figure 2B.

Similar to the commercial applications, TAAL-1 processors 130, 135 demultiplex tactical CVSD voice or data calls and place a single 16 or 32 kb/s CVSD voice or data call (or a group of N multiplexed 16 or 32 kb/s CVSD calls) into 384 bit segments. Figure 9 shows a diagram of a TAAL-1 cell 900 consistent with this invention. The first eight bits of cell 900 constitute the TAAL-1 header 910, and the succeeding 376 bits contain CVSD information (or data) 920. TAAL-1 header 910 includes: (1) the CSI (Convergence Sublayer Indicator), which is set to 0 for TAAL-1; (2) SN (Sequence Number), which is the Modulo 8 count computed and inserted by the source TAAL-1 process, used by the receiving endpoint to determine if cells have been lost; (3) CRC (Cyclic Redundancy Check), which is computed and inserted by the source TAAL-1 process across the CSI and SN bits, used by the receiving endpoint for error detection and 1-bit correction of CSI and SN, in conjunction with the P bit; and (4) parity, which is the even parity bit computed and inserted by the source TAAL-1 process across the 7-bit codeword, consisting of CSI, SN, and CRC.

TAAL-1 processors 130, 135 allow a single voice or data channel per cell or multiple (time-synchronized TDM) voice or data channels per cell. Those processors also allow tandem ATM switching of cells carrying voice or data, and provide one AAL process per virtual circuit. In addition, during periods of cell loss at the TAAL-1 reassembler, or during buffer underflow, fill data appropriate to the type of calls being supported is played out to TDM users.

TAAL-1 processors 130, 135 for CVSD voice interfaces to two 1024 channel groups, and each channel can operate at 16, 32, or 64 Kbps carrying CVSD voice, PCM voice or data. The two 1024 channel groups are demultiplexed, and up to 400 of these channels can be dynamically selected for individual encapsulation into cells using a TAAL-1. In addition, groups of these time slots, up to 47, can be encapsulated within a single cell stream (AAL process). Each TAAL-1 process is dynamically configured based on the data rate of the source channel or channels (16, 32, or 64 Kbps) to operate at the proper rate. Up to forty-seven bytes of data can be encapsulated into a single cell, each byte corresponding to a channel on the source 1024 channel groups. Each channel multiplexed within a single cell stream (a single AAL process) must be operating at the same data rate. Individual channels can be repeated within a specific cell, and if more than one channel is assigned to a cell stream (AAL process), the repetitive pattern of channels is not allowed to span multiple cells because the TAAL-1 does not use a Structure Pointer. Instead of a Structure Pointer, the TAAL-1 uses octet alignment within the cell payload to delineate a multiple channel structure for use when assembling information for the transmission.

The Structure Pointer defined for commercial AAL1 is not protected by any sort of error detection or correction and is therefore subject to undetected corruption in a high Bit Error Rate (BER) environment. In addition, under high cell loss situations, a commercial AAL will lose synchronization with the source and have to reacquire the Structure Pointer before getting back in sync which means frequent periods of lost data. The TAAL-1 ensures that the structure is repeated consistently in every cell so that it does not need to rely on any sort of pointer mechanism to guarantee that the receiving end can reassemble the cell stream and multiplex the channels into the proper positions on the 1024 channel groups. The

TAAL-1 therefore does not suffer from any loss of synchronization problems like the commercial AAL1.

Since cell delay variation (CDV) is small in commercial networks, commercial AAL1 implementations typically use small reassembly buffers. These reassembly buffers are designed to absorb CDV in the microsecond to very low millisecond range. In the tactical environment, CDVs can be large, sometimes up to almost 200 ms. The TAAL-1 implementation was designed specifically to handle the wide variation of expected CDVs, from the very small commercial like values all the way up to the worst case tactical values.

In addition, commercial implementations of AAL1 do not typically allow selection of the fill pattern played from the reassembly process when there is a lost cell or cell starvation. Commercial implementations use a default which is not user-selectable. The TAAL-1 allows individual selection of a repetitive eight-bit pattern for each of the up to 400 AALs. The fill pattern can therefore be selected appropriately based on the nature of the source data to be encapsulated.

In one embodiment, a single card can support 400 independent AAL processes running simultaneously with up to 47 TDM channels per cell and a dual TDM interface. There can be a sixteen cell reassembly buffers per AAL process, expandable to 128; a fast AAL sequence number algorithm; and no need for a structure pointer. There is also a dynamically-configurable fill pattern per AAL process and elastic buffering per AAL process. In addition, systems consistent with this invention support variable cell utilization (partially filled cells method) per AAL process, and 16 kb/s CVSD, 32 kb/s CVSD, and/or 64 kb/s PCM operation simultaneously. Also, the TAAL-1 header is protected by powerful error control coding, *e.g.*, the (82, 40) binary BCH code.

CONCLUSION

Persons of ordinary skill in the art will recognize that various modifications and variations can be made in the methods and apparatuses of the present invention without departing from the scope or spirit of the invention.

Other embodiments of the invention will be apparent to those skilled in the art from consideration of the specification and practice of the invention. The specification and

examples are only exemplary. The true scope and spirit of the invention is indicated by the following claims.

Claims

1. A method of creating a frame containing tactical payload data comprising the steps, executed by a data processor, of:

placing a portion of the payload data into a fixed size tactical payload portion of a cell in the frame;

forming a tactical fixed size header portion of the cell containing routing information for the cell; and

appending a synchronization character to the cell.

2. The method of claim 1, wherein the step of placing the portion of the payload into the payload portion of the cell includes the substep of

using forty bits of the header position for header information.

3. The method of claim 1, wherein the step of forming the tactical fixed size header portion includes the substep of

placing the header into forty bits of the header portion.

4. The method of claim 1, wherein the step of forming the tactical fixed size header portion includes the substep of

placing eight bits of the payload into the header portion.

5. The method of claim 1, wherein the step of appending the synchronization character includes the substep of

inserting a five-bit synchronization character.

6. The method of claim 5, wherein the step of appending the synchronization character includes the substep of

placing a different synchronization character on alternate frames.

7. The method of claim 6, wherein the substep of placing different synchronization characters on alternate frames includes the substep of

using five-bit synchronization characters.

8. The method of claim 7, wherein the substep of using five-bit synchronization characters includes the substep of

using 10001 and 01110 as synchronization characters.

9. The method of claim 4, further including the step of

encoding the header portion of the cell separately from the payload portion using a first error detecting/correcting code.

10. The method of claim 9, further including the step of

encoding the payload portion of the cell with a second error detecting/correcting code different from the first code.

11. The method of claim 10, further including the step of

encoding the payload portion of the cell with a (421,376) BCH error detecting/correcting code.

12. The method of claim 9, wherein the step of encoding the header portion of the cell includes the substep of

using a (82,40) BCH code.

13. A method of creating a tactical ATM frame from an ATM cell having header data with error detecting/correcting codes and payload data, the method comprising the steps, executed by a data processor, of:

placing into a header portion of the frame the header data from the ATM cell other than the error detecting/correcting codes;

placing a portion of the payload data from the ATM cell into the header portion of the frame;

placing the remainder of payload data into a payload portion the frame; and

appending a synchronization character to the cell.

14. The method of claim 13, wherein the step of placing the portion of the payload data into the payload portion of the cell includes the substep of

placing 376 bits of the payload data into the payload portion.

15. The method of claim 13, wherein the step of placing header data into the header portion of the frame includes the substep of

placing thirty-two bits of the header data into forty bits of the header portion.

16. The method of claim 13, wherein the step of placing a portion of the payload data from the ATM cell into the header portion of the frame includes the substep of

placing eight bits of the payload data into the header portion.

17. The method of claim 13, wherein the step of appending the synchronization character includes the substep of

inserting a five-bit synchronization character.

18. The method of claim 17, wherein the step of appending the synchronization character includes the substep of

placing a different synchronization character on alternate frames.

19. The method of claim 18, wherein the substep of placing different synchronization characters on alternate frames includes the substep of

using five-bit synchronization characters.

20. The method of claim 19 wherein the substep of using five-bit synchronization characters includes the substep of

using 10001 and 01110 as synchronization characters.

21. The method of claim 13, further including the step of

encoding the header portion separately from the payload portion using a first error detecting/correcting code.

22. The method of claim 21, further including the step of

encoding the payload portion of the cell with a second error detecting/correcting code different from the first code.

23. The method of claim 22, further including the step of

encoding the payload portion with a (421,376) BCH error detecting/correcting code.

24. The method of claim 21, wherein the step of encoding the header portion includes the substep of

using a (82,40) BCH code.

25. An encoder for building a frame containing tactical payload data comprising:

means for placing a portion of the payload data into a fixed-size tactical payload portion of a cell in the frame;

means for forming a tactical fixed size header portion of the cell containing routing information for the cell; and

means for appending a synchronization character to the cell.

26. The encoder of claim 25, wherein the means for placing the portion of the payload into the payload portion of the cell includes

means for placing 376 bits of the payload in the payload portion.

27. The encoder of claim 25, wherein the means for forming the tactical fixed size header portion of the cell includes

means for placing header data into forty bits of the header portion.

28. The encoder of claim 25, wherein the means for forming the tactical fixed size header portion of the cell includes

means for placing eight bits of the payload into the header portion.

29. The method of claim 25, wherein the means for appending the synchronization character includes

means for inserting a five-bit synchronization character.

30. The method of claim 29, wherein the means for appending the synchronization character includes

means for placing a different synchronization character on alternate ones of the frames.

31. The method of claim 30, wherein the means for placing different synchronization characters on alternate frames includes

means for using five-bit synchronization characters.

32. The method of claim 31, wherein the means for using five-bit synchronization characters includes

means for using 10001 and 01110 as synchronization characters.

33. The encoder of claim 25, further including

means for encoding the header portion of the cell separately from the payload portion using a first error detecting/correcting code.

34. The encoder of claim 33, further including

means for encoding the payload portion of the cell with a second error detecting/correcting code different from the first code.

35. The encoder of claim 34, further including

means for encoding the payload portion of the cell with a (421,376) BCH error detecting/correcting code.

36. The encoder of claim 30, wherein the means for encoding the header portion of the cell includes

means for using a (82,40) BCH code.

37. An encoder for creating a tactical ATM frame from an ATM cell having header data with error detecting/correcting codes and payload data comprising:

means for receiving the ATM cell;

means for transferring into a header portion of the frame the header data from the ATM cell other than the error detecting/correcting codes;

means for transferring a portion of the payload data from the ATM cell into the header portion of the frame;

means for transferring the remainder of payload data into a payload portion of the frame; and

means for appending a synchronization character to the cell.

38. The encoder of claim 37 wherein the means for transferring the portion of the payload data into the payload portion of the cell includes

means for placing 376 bits of the payload data into the payload portion.

39. The encoder of claim 37 wherein the means for transferring header data into the header portion of the frame includes

means for placing thirty-two bits of the header data into forty bits of the header portion.

40. The encoder of claim 37, wherein the means for transferring a portion of the payload data from the ATM cell into the header portion of the frame includes

means for placing eight bits of the payload data into the header portion.

41. The encoder of claim 37, wherein the means for appending the synchronization character includes the substep of

means for inserting a five-bit synchronization character.

42. The encoder of claim 41, wherein the means for appending the synchronization character includes

means for placing a different synchronization character on alternate frames.

43. The encoder of claim 42, wherein the substep of placing different synchronization characters on alternate frames includes

means for using five-bit synchronization characters.

44. The encoder of claim 43, wherein the means for using five-bit synchronization characters includes

means for using 10001 and 01110 as synchronization characters.

45. The encoder of claim 37, further including

means for encoding the header portion separately from the payload portion using a first error detecting/correcting code.

46. The encoder of claim 45, further including

means for encoding the payload portion of the cell with a second error detecting/correcting code different from the first code.

47. The encoder of claim 46, further including

means for encoding the payload portion with a (421,376) BCH error detecting/correcting code.

48. The encoder of claim 45, wherein the means for encoding the header portion includes

means for using a (82,40) BCH code.

49. The encoder of claim 45, wherein the means for encoding the header portion includes

a header parity generator

50. The encoder of claim 49, wherein the header parity generator includes

a linear-feedback, 42-bit shift register.

51. The encoder of claim 46, wherein the means for encoding the payload portion includes

a payload parity generator.

52. The encoder of claim 51 wherein the payload parity generator includes

a 45-bit linear feedback shift register.

53. The encoder of claim 37, further including

means for interleaving the header portion and the payload portion.

54. The encoder of claim 53, wherein the means for interleaving includes

control circuitry, and

a multiplexer, receiving data from the header portion and the payload portion and responsive to the control circuitry to interleave bits from the header portion with bits from the payload portion.

55. A method of creating a frame containing tactical payload data comprising the steps, executed by a data processor, of:

placing a portion of the payload data into a fixed size tactical portion of a cell in the frame;

forming a tactical fixed size header portion of the cell containing routing information for the cell; and

encoding the header portion of the cell separately from the payload portion using a first error detecting/correcting code.

56. The method of claim 55, further including the step of

encoding the payload portion of the cell with a second error detecting/correcting code different from the first code.

57. The method of claim 55, wherein the step of placing the portion of the payload in a fixed size tactical portion of the cell includes the substep of

placing the 376 bits of the payload in the payload portion.

58. The method of claim 57, further including the step of

encoding the payload portion of the cell with a (421,376) BCH error detecting/correcting code.

59. The method of claim 57, wherein the step of placing the header in a fixed size tactical portion of the cell includes the substep of

placing the header into forty bits of the header portion.

60. The method of claim 59, wherein the step of encoding the header portion of the cell includes the substep of

using a (82,40) BCH code.

61. The method of claim 59, wherein the step of forming a tactical fixed size header portion includes the substep of

placing eight bits of the payload into the header portion.

62. An encoder for building a frame containing tactical payload data comprising:

means for placing a portion of the payload data into a fixed size tactical portion of a cell in the frame;

means for forming a tactical fixed size header portion of the cell containing routing information for the cell; and

means for encoding the header portion of the cell separately from the payload portion using a first error detecting/correcting code.

63. The encoder of claim 62, further including

means for encoding the payload portion of the cell with a second error detecting/correcting code different from the first code.

64. The encoder of claim 62, wherein the means for placing the portion of the payload in a fixed size tactical portion of the cell includes

means for placing the 376 bits of the payload in the payload portion.

65. The encoder of claim 63, further including

means for encoding the payload portion of the cell with a (421,376) BCH error detecting/correcting code.

66. The encoder of claim 62, wherein the means for placing the header in a fixed size tactical portion of the cell includes

means for placing the header into forty bits of the header portion.

67. The encoder of claim 66, wherein the means for encoding the header portion of the cell includes

means for using a (82,40) BCH code.

68. The encoder of claim 66. wherein the means for forming a tactical fixed size header portion includes

means for placing eight bits of the payload into the header portion.

69. A method of flexibly encoding a portion of a tactical cell for transmission on a channel, comprising the steps of:

selecting an error detection/correction code to match transmission characteristics of the channel;

setting an encoder to implement the error detection/correction code on the portion of the cell by

storing generator polynomial coefficients representing the selected error detection/correction code, and

shifting in information bits of the tactical cell portion; and

forming combinations of the information bits based on the coefficients to encode the tactical cell portion with the selected error detection/correction code.

70. The method of claim 69, wherein the step of selecting the error detection/correction code includes the substep of

determining the quality of the channel.

71. The method of claim 70. wherein the step of selecting the error detection/correction code includes the substep of

decreasing the number of coefficients if the quality of the channel deteriorates.

72. The method of claim 70. wherein the step of selecting the error detection/correction code includes the substep of

increasing the number of coefficients if the quality of the channel deteriorates.

73. The method of claim 70, wherein the step of selecting the error detection/correction code includes the substep of

decreasing a number of parity check bits if the quality of the channel improves.

74. The method of claim 70. wherein the step of selecting the error detection/correction code includes the substep of

decreasing the number of coefficients if the quality of the channel improves.

75. The method of claim 69, wherein the step of receiving feedback indicating the quality of the channel includes the substep of

receiving a message indicating the average number of number of errors corrected.

76. The method of claim 75, wherein the step of selecting the error detection/correction code includes the substep of

decreasing the number of coefficients as the number of errors decreases.

77. The method of claim 75, wherein the step of selecting the error detection/correction code includes the substep of

increasing the number of coefficients as the number of errors increases.

78. The method of claim 75, wherein the step of selecting the error detection/correction code includes the substep of

increasing a number of parity bits if the number of errors increases.

79. The method of claim 75, wherein the step of selecting the error detection/correction code includes the substep of

decreasing the number of coefficients as the number of errors increases.

80. The method of claim 75, wherein the step of selecting the error detection/correction code includes the substep of

using a binary BCH code.

81. An encoder for flexibly encoding a portion of a tactical cell for transmission on a channel, comprising:

means for selecting an error detection/correction code to match transmission characteristics of the channel;

means for setting an encoder to implement the error detection/correction code on the portion of the cell by

means for storing generator polynomial coefficients representing the selected error detection/correction code, and

means for shifting in information bits of the tactical cell portion; and

means for forming combinations of the information bits based on the coefficients to encode the tactical cell portion with the selected error detection/correction code.

82. The encoder of claim 81, wherein the means for selecting the error detection/correction code includes

means for determining the quality of the channel.

83. The encoder of claim 82, wherein the means for selecting the error detection/correction code includes

means for decreasing the number of coefficients if the quality of the channel deteriorates.

84. The encoder of claim 82, wherein the step of selecting the error detection/correction code includes

means for increasing the number of coefficients if the quality of the channel deteriorates.

85. The encoder of claim 82, wherein the means for selecting the error detection/correction code includes

means for decreasing a number of parity check bits if the quality of the channel improves.

86. The encoder of claim 82, wherein the means for selecting the error detection/correction code includes

means for decreasing the number of coefficients if the quality of the channel improves.

87. The encoder of claim 81, wherein the step of receiving feedback indicating the quality of the channel includes

means for receiving a message indicating the average number of number of errors corrected.

88. The encoder of claim 87, wherein the means for selecting the error detection/correction code includes

means for decreasing the number of coefficients as the number of errors decreases.

89. The encoder of claim 87, wherein the means for selecting the error detection/correction code includes

means for increasing the number of coefficients as the number of errors increases.

90. The encoder of claim 87, wherein the means for selecting the error detection/correction code includes

means for increasing a number of parity bits if the number of errors increases.

91. The encoder of claim 87, wherein the means for selecting the error detection/correction code includes

means for decreasing the number of coefficients as the number of errors increases.

92. The encoder of claim 81, wherein the means for selecting the error detection/correction code includes

means for using a binary BCH code.

93. A method of decoding a tactical cell, comprising the steps of:

deriving circuits and tables from a primitive polynomial;

computing syndromes of a received word using a plurality of the circuits:

finding an error locator polynomial from the syndromes using the tables;

finding roots of the error locator polynomial using a plurality of circuits; and

correcting any errors by applying the error locator polynomial to the received word.

94. The method of claim 93, wherein the step of computing the syndromes includes the substep of

shifting the received word into t generalized shift registers, where t is the maximum number of errors correctable by the code.

95. The method of claim 94, wherein the substep of shifting the received word into t generalized shift registers further includes the substep of

shifting the received word through m stages of the shift registers, where the maximum block length of the code is $2^m - 1$.

96. The method of claim 93, wherein the step of finding the error locator polynomial includes the substep of

performing a Chien search.

97. The method of claim 96, wherein the substep of performing a Chien search further includes the substep of

shifting the received word into t generalized shift registers, where t is the maximum number of errors correctable by the code.

98. The method of claim 97, wherein the substep of shifting the received word into t generalized shift registers further includes the substep of

shifting the received word through m stages of the shift registers, where the maximum block length of the code is $2^m - 1$.

99. The method of claim 93, wherein the step of finding the roots of the error locator polynomial includes the substep of

performing a Massey algorithm.

100. The method of claim 99, wherein the substep of performing the Massey algorithm further includes the substep of

generating a table of m-tuples representing $GF(2^m)$, where the maximum block length of the code is $2^m - 1$.

101. The method of claim 99, further including the step of

initializing the Massey algorithm with the number of errors to be corrected, the degree of the primitive polynomial, the coefficients of the primitive polynomial, and the length of the cell.

102. A decoder comprising:

means for deriving circuits and tables from a primitive polynomial;

means for computing syndromes of a received word using a plurality of the circuits;

means for finding an error locator polynomial from the syndromes using the tables;

means for finding roots of the error locator polynomial using a plurality of circuits; and

means for correcting any errors by applying the error locator polynomial to the received word.

103. The decoder of claim 102, wherein the means for computing the syndromes includes t shift registers, where t is the maximum number of errors correctable by the code.

104. The decoder of claim 103, wherein the shift registers each include m stages of the shift registers, where the maximum block length of the code is $2^m - 1$.

105. The decoder of claim 103, wherein the shift registers are integrated in an ASIC.

106. The decoder of claim 102, wherein the means for finding the error locator polynomial includes

a Chien search engine.

107. The decoder of claim 106, wherein the Chien search engine further includes

t shift registers, where t is the maximum number of errors correctable by the code.

108. The decoder of claim 107, wherein the shift registers each include

m stages of the shift registers, where the maximum block length of the code is 2^m -1.

109. The decoder of claim 108, wherein the shift registers are integrated in an ASIC.

110. The decoder of claim 102, wherein the means for finding the roots of the error locator polynomial includes

a Massey algorithm processor.

111. The decoder of claim 110, wherein the Massey algorithm processor includes

a table of m-tuples representing GF(2^m), where the maximum block length of the code is 2^m -1.

112. The decoder of claim 110, further including

means for initializing the Massey algorithm processor with the number of errors to be corrected, the degree of the primitive polynomial, the coefficients of the primitive polynomial, and the length of the cell.

113. The decoder of claim 110, wherein the Massey algorithm processor is integrated in an ASIC.

114. A method for transmitting a frame containing tactical payload data bits and header bits, comprising the steps, executed by a data processor, of:

interleaving the header bits and the payload bits by inserting a header bit after a first number of payload bits; and

transmitting the interleaved header bits and payload bits.

115. The method of claim 114, wherein the interleaving step includes the substep of

placing additional payload bits after the interleaved header and payload bits.

116. The method of claim 114, wherein there are eighty-two header bits and 421 payload bits, and wherein the interleaving step includes the substep of

alternating four payload bits and one header bit.

117. The method of claim 116, further including the step of

placing 93 payload bits after the last header bit.

118. The method of claim 114, wherein there are eighty-two header bits and 376 payload bits, and wherein the interleaving step includes the substep of

alternating four payload bits and one header bit.

119. The method of claim 116, further including the step of

placing 48 payload bits after the last header bit.

120. The method of claim 114, further including the step of

appending a synchronization character to the cell.

121. The method of claim 120, wherein the step of appending a synchronization character includes the substep of

appending a five-bit synchronization character.

122. The method of claim 120, wherein the step of appending a synchronization character includes the substep of

appending a synchronization character that has alternating values.

123. An apparatus for transmitting a frame containing tactical payload data bits and header bits, comprising:

means for interleaving the header bits and the payload bits by inserting a header bit after a first number of payload bits;

means for transmitting the interleaved header bits and payload bits.

124. The apparatus of claim 123, wherein the interleaving means includes

a multiplexer.

125. The apparatus of claim 123, wherein the means for interleaving includes

means for placing additional payload bits after the interleaved header and payload bits.

126. The apparatus of claim 123, wherein there are eighty-two header bits and 421 payload bits, and wherein the means for interleaving includes

means for alternating four payload bits and one header bit.

127. The apparatus of claim 126, further including

means for placing 93 payload bits after the last header bit.

128. The apparatus of claim 123, wherein there are eighty-two header bits and 376 payload bits, and wherein the means for interleaving includes

means for alternating four payload bits and one header bit.

129. The apparatus of claim 126, further including

means for placing 48 payload bits after the last header bit.

130. The apparatus for claim 123, further including

means for appending a synchronization character to the cell.

131. The apparatus of claim 130, wherein the step of appending a synchronization character includes the means for

appending a five-bit synchronization character.

132. The apparatus of claim 130, wherein the means for appending a synchronization character includes

means for appending a synchronization character that has alternating values.

133. A method of creating a frame containing tactical payload data comprising the steps, executed by a data processor, of:

placing a portion of the payload data into a fixed size tactical payload portion of a cell in the frame;

forming a tactical fixed size header portion of the cell containing routing information for the cell; and

appending a synchronization character to the cell that takes alternating values.

134. The method of claim 133, wherein the step of appending the synchronization character includes the substep of

inserting five-bit synchronization characters.

135. The method of claim 134, wherein the substep of using five-bit synchronization characters includes the substep of

using 10001 and 01110 as synchronization characters.

136. The method of claim 133, wherein the step of forming a tactical fixed size header portion of the cell includes the substep of

extracting the header from an ATM cell.

137. The method of claim 133, wherein the step of placing a portion of the payload data into a fixed size tactical payload portion of a cell includes the substep of

extracting the payload from an ATM cell.

138. A method of decoding frames containing synchronization characters and header portions, comprising the steps, executed by a data processor, of:

detecting a first synchronization character for a first frame;

detecting a second synchronization character for a second frame following the first frame in succession;

forming a hypothesis about the construction of at least one of the frames:

locating a header portion in one of the frames according to the hypothesis:

decoding the header portion; and

declaring successful framing if the synchronization characters are detected and the header portion is successfully decoded.

139. The method of claim 138, further including the step of

starting the method over if the synchronization characters are detected and the header portion is successfully decoded.

140. The method of claim 138, wherein the step of a detecting the second synchronization character includes the substep of

detecting the second synchronization character that is different from the first synchronization character.

141. The method of claim 140, wherein the step of detecting a first synchronization character includes the substep of

detecting a character of 10001, and

wherein the step of detecting the second synchronization character includes the substep of

detecting a character of 01110.

142. An encoder for creating a frame containing tactical payload data comprising the steps, executed by a data processor, of:

means for placing a portion of the payload data into a fixed size tactical payload portion of a cell in the frame;

means for forming a tactical fixed size header portion of the cell containing routing information for the cell; and

means for appending a synchronization character to the cell that takes alternating values.

143. The encoder of claim 142, wherein the means for appending the synchronization character includes

means for inserting five-bit synchronization characters.

144. The encoder of claim 134, wherein the means for using five-bit synchronization characters includes

means for using 10001 and 01110 as synchronization characters.

145. The encoder of claim 142, wherein the means for forming a tactical fixed size header portion of the cell includes

means for extracting the header from an ATM cell.

146. The encoder of claim 142, wherein the step of placing a portion of the payload data into a fixed size tactical payload portion of a cell includes

means for extracting the payload from an ATM cell.

147. A decoder for detecting frames containing synchronization characters and header portions, comprising:

means for detecting a first synchronization character for a first frame;

means for detecting a second synchronization character for a second frame following the first frame in succession;

means for forming a hypothesis about the construction of at least one of the frames;

means for locating a header portion in one of the frames according to the hypothesis;

means for decoding the header portion; and

means for declaring successful framing if the synchronization characters are detected and the header portion is successfully decoded.

148. The decoder of claim 147, further including

means for starting the method over if the synchronization characters are detected and the header portion is successfully decoded.

149. The decoder of claim 147, wherein the means for detecting the second synchronization character includes

means for detecting the second synchronization character that is different from the first synchronization character.

150. The decoder of claim 149, wherein the means for detecting a first synchronization character includes

means for detecting a character of 10001, and

wherein the means for detecting the second synchronization character includes

means for detecting a character of 01110.

151. A method of converting a high layer transmission into a format compatible with a tactical cell comprising the steps, executed by a data processor, of:

multiplexing the transmission into tactical payload data;

forming a header for use when reassembling information for the transmission;

placing a portion of the payload data into a fixed size tactical payload portion of a cell;

forming a tactical fixed size header portion for the cell containing routing information; and

setting a synchronization character to the cell.

152. The method of claim 151, further including the step of

supporting variable cell utilization for each cell.

153. The method of claim 151, wherein the placing step includes the substep of protecting the header by a (82,40) ATM cell header codeword.

154. The method of claim 151, wherein there are 400 independent AAL (ATM adaptation layer) processes running simultaneously, and further including the step of

using a dual TDM (time division multiplexed) interface.

155. The method of claim 154, further including the step of

utilizing up to forty-seven TDM channels per cell.

156. A converter for modifying a high layer transmission into a format compatible with a tactical cell comprising:

means for multiplexing the transmission into tactical payload data;

means for forming a header for use when reassembling information for the transmission;

means for placing a portion of the payload data into a fixed size tactical payload portion of a cell;

means for forming a tactical fixed size header portion for the cell containing routing information; and

means for setting a synchronization character to the cell.

157. The converter of claim 156, further including

means for supporting variable cell utilization for each cell.

158. The converter of claim 156, wherein the means for placing further includes

means for protecting the header by a (82,40) ATM cell header codeword.

159. The converter of claim 156, wherein there are 400 independent AAL (ATM adaptation layer) processes running simultaneously, and further including

means for using a dual TDM (time division multiplexed) interface.

160. The converter of claim 159, further including

means for utilizing up to forty-seven TDM channels per cell.

161. A method of converting a high layer transmission into a format compatible with a tactical cell comprising the steps, executed by a data processor, of:

demultiplexing a transmission into tactical payload data;

placing a portion of the payload data into a fixed size tactical payload portion of a cell;

forming a header for use when reassembling information for the transmission;

forming a tactical fixed size header portion for the cell containing routing information;

setting a synchronization character to the cell.

162. The method of claim 161, further including the step of

supporting variable cell utilization for each cell.

163. The method of claim 161, wherein the placing step includes the substep of protecting the header by a (82,40) ATM cell header codeword.

164. The method of claim 161, wherein there are 400 independent AAL (ATM adaptation layer) processes running simultaneously, and further including the step of using a dual TDM (time division multiplexed) interface.

165. The method of claim 164, further including the step of utilizing up to forty-seven TDM channels per cell.

166. A converter for modifying a high layer transmission into a format compatible with a tactical cell comprising:

means for demultiplexing a transmission into tactical payload data;

means for placing a portion of the payload data into a fixed size tactical payload portion of a cell;

means for forming a header for use when reassembling information for the transmission;

means for forming a tactical fixed size header portion for the cell containing routing information;

means for setting a synchronization character to the cell.

167. The converter of claim 166, further including means for supporting variable cell utilization for each cell.

168. The converter of claim 166, wherein the means for placing further includes means for protecting the header by a (82,40) ATM cell header codeword.

169. The converter of claim 166, wherein there are 400 independent AAL (ATM adaptation layer) processes running simultaneously, and further including means for using a dual TDM (time division multiplexed) interface.

170. The converter of claim 169, further including means for utilizing up to forty-seven TDM channels per cell.

171. A method of flexibly encoding and decoding a portion of a tactical frame for transmission on a channel, comprising the steps of:

selecting error detection/correction codes to match transmission characteristics of the channel;

setting an encoder to implement the selected error detection/correction code on a portion of a cell by

storing a generator polynomial of the selected error detection/correction code; and

setting a decoder to implement the selected error detection/correction code on a portion of the cell by

storing a maximum number of errors to be corrected, and

storing a primitive polynomial of the selected error detection/correction code.

172. The method of claim 171, wherein the step of selecting the error detection/correction code includes the substep of

changing the generator polynomials to polynomials with larger degree if the quality of the channel deteriorates.

173. The method of claim 171, wherein the step of selecting the error detection/correction code includes the substep of

increasing the maximum number of errors to be corrected by the decoders if the quality of the channel deteriorates.

174. The method of claim 171, wherein the step of selecting the error detection/correction code includes the substep of

changing the generator polynomials to polynomials with smaller degree if the quality of the channel improves.

175. The method of claim 171, wherein the step of selecting the error detection/correction code includes the substep of

decreasing the maximum number of errors to be corrected by the decoders if the quality of the channel improves.

176. The method of claim 171, wherein the step of receiving feedback indicating the quality of the channel includes the substep of

receiving a message indicating the average number of number of errors corrected per frame.

177. The method of claim 176, wherein the step of selecting the error detection/correction code includes the substep of

decreasing the maximum number of errors corrected by the decoders if the average number of errors corrected per cell decreases sufficiently.

178. The method of claim 176, wherein the step of selecting the error detection/correction code includes the substep of

increasing the maximum number of errors corrected by the decoders if the average number of errors corrected per frame increases sufficiently or if the number of decoding failures of the header code increases sufficiently.

179. The method of claim 176, wherein the step of selecting the error detection/correction code includes the substep of

changing the generator polynomials to polynomials with smaller degree if the average number of errors corrected per frame decreases sufficiently.

180. The method of claim 176, wherein the step of selecting the error detection/correction code includes the substep of

changing the generator polynomials to polynomials with larger degree if the average number of errors corrected per frame increases sufficiently or if the number of decoding failures increases sufficiently.

181. An encoder/decoder for flexibly encoding and decoding a portion of a tactical cell for transmission on a channel, comprising:

means for selecting an error detection/correction code to match transmission characteristics of the channel;

means for applying the error detection/correction code to the portion of the cell including

means for storing the code generator polynomials, and

means for storing the maximum number of errors to be corrected, and

means for storing the primitive polynomials.

182. The encoder/decoder of claim 181, wherein the means for selecting the error detection/correction code includes

means for decreasing the maximum numbers of errors corrected if the channel conditions improve.

183. The encoder/decoder of claim 181, wherein the step of selecting the error detection/correction code includes

means for increasing the maximum number of errors corrected if the quality of the channel deteriorates.

184. The encoder/decoder of claim 181, wherein the means for selecting the error detection/correction code includes

means for changing the generator polynomials of the codes to polynomials with smaller degree if the quality of the channel improves.

185. The encoder/decoder of claim 181, wherein the means for selecting the error detection/correction code includes

means for changing the generator polynomials of the codes to polynomials with larger degree if the quality of the channel deteriorates.

186. The encoder/decoder of claim 181, wherein the step of receiving feedback indicating the quality of the channel includes

means for receiving a message indicating the average number of number of errors corrected per frame and the number of decoding failures.

187. The encoder/decoder of claim 181, wherein the means for selecting the error detection/correction code includes

means for decreasing the maximum numbers of errors corrected as the average number of errors corrected per frame decreases.

188. The encoder/decoder of claim 187, wherein the means for selecting the error detection/correction code includes

means for increasing the maximum number of errors corrected as the average number of errors per frame increases or the number of decoding failures increases.

189. The encoder/decoder of claim 187, wherein the means for selecting the error detection/correction code includes

means for changing the generator polynomials of the codes to polynomials of smaller degree as the average number of errors corrected per frame decreases.

190. The encoder/decoder of claim 187, wherein the means for selecting the error detection/correction code includes

means for changing the generator polynomials of the codes to polynomials of larger degree as the average number of errors corrected per frame increases or the number of decoding failures increases.

191. A method of decoding a tactical cell, comprising the steps of:

computing syndromes from a received word;

finding an error locator polynomial form the syndromes;

finding roots of the error locator polynomial; and

correcting any errors by applying the error locator polynomial to the received word.

192. The method of claim 191, wherein the step of computing a syndrome includes the substep of

shifting the received word into t generalized shift registers, where t is the maximum number of errors correctable by the code.

193. The method of claim 191, wherein the step of computing the syndromes includes the substep of

shifting the received word into 2t generalized shift registers, where 2t is the maximum number of errors correctable by the code.

194. A decoder comprising:

means for computing syndromes of a received word;

means for finding an error locator polynomial from the syndromes;

means for finding roots of the error locator polynomial; and

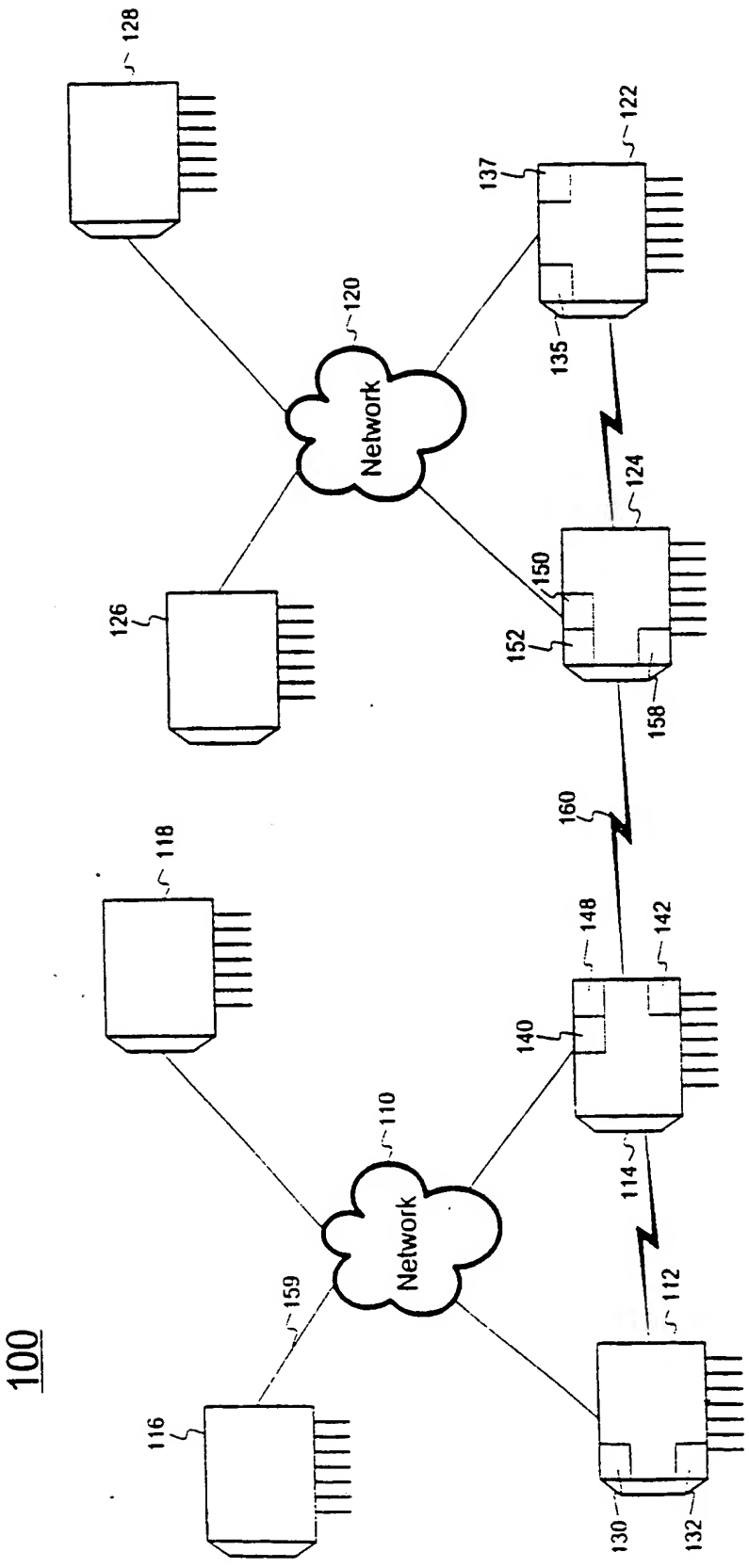
means for correcting any errors by applying the error locator polynomial to the received word.

195. The decoder of claim 194, wherein the means for computing a syndrome includes

t shift registers, where t is the maximum number of errors correctable by the code.

196. The decoder of claim 194, wherein the shift registers each include 2t shift registers, where 2t is the maximum number of errors correctable by the code.

Figure 1


100
128
122
137
120
Network
135
124
126
150
152
158
160
118
148
142
140
110
Network
114
112
159
116
130
132

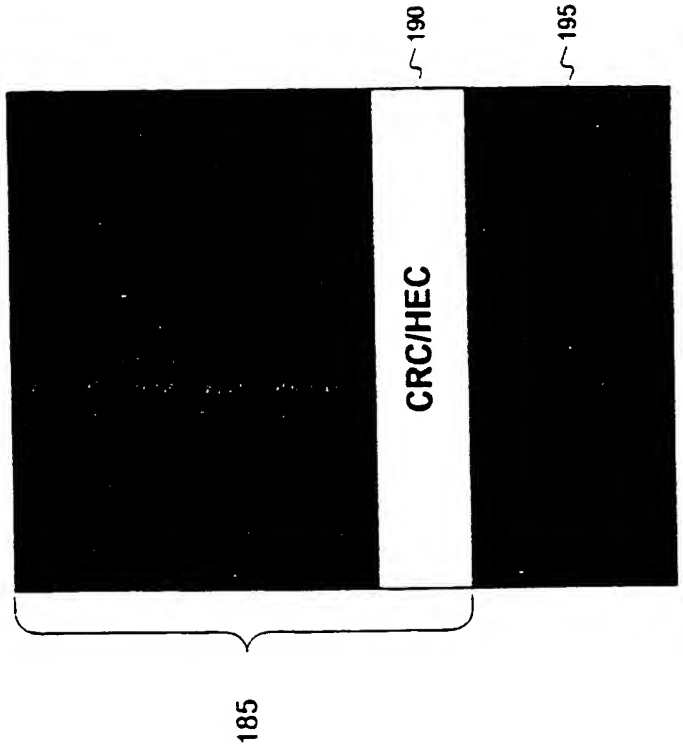


Figure 2A

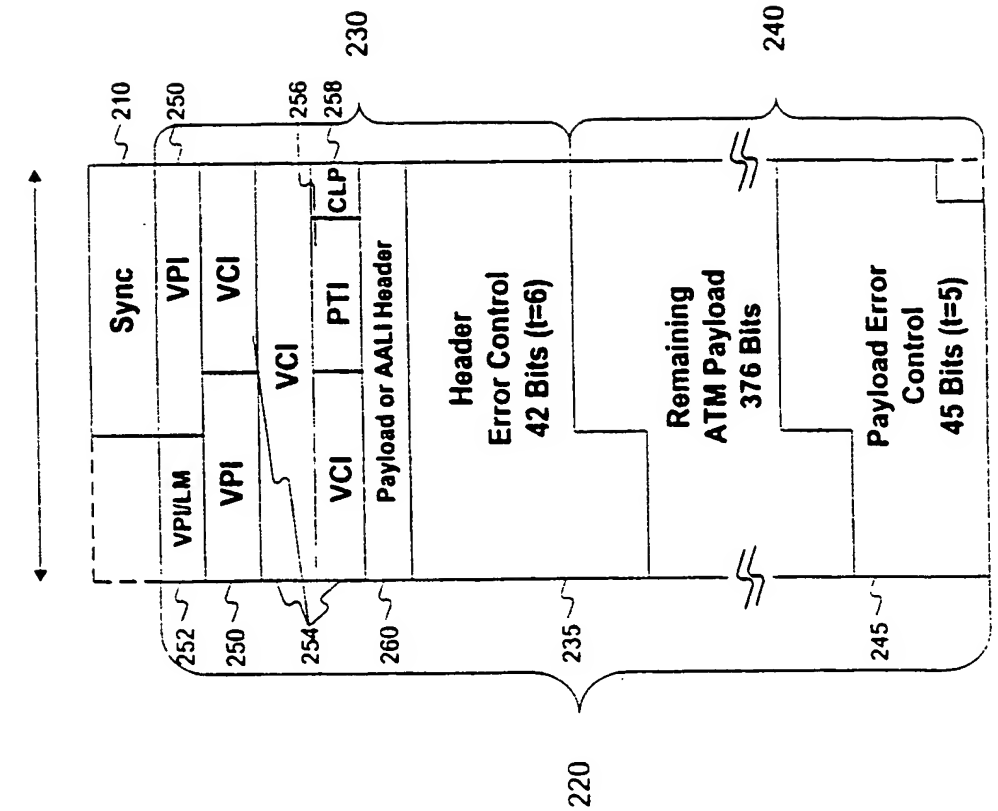

200
210
250
256
258
230
240
Sync
VPI
VCI
VCI
PTI
CLP
VPI/LM
VPI
VCI
Payload or AALI Header
Header Error Control 42 Bits (t=6)
Remaining ATM Payload 376 Bits
Payload Error Control 45 Bits (t=5)
252
250
254
260
235
245
220

Figure 2B

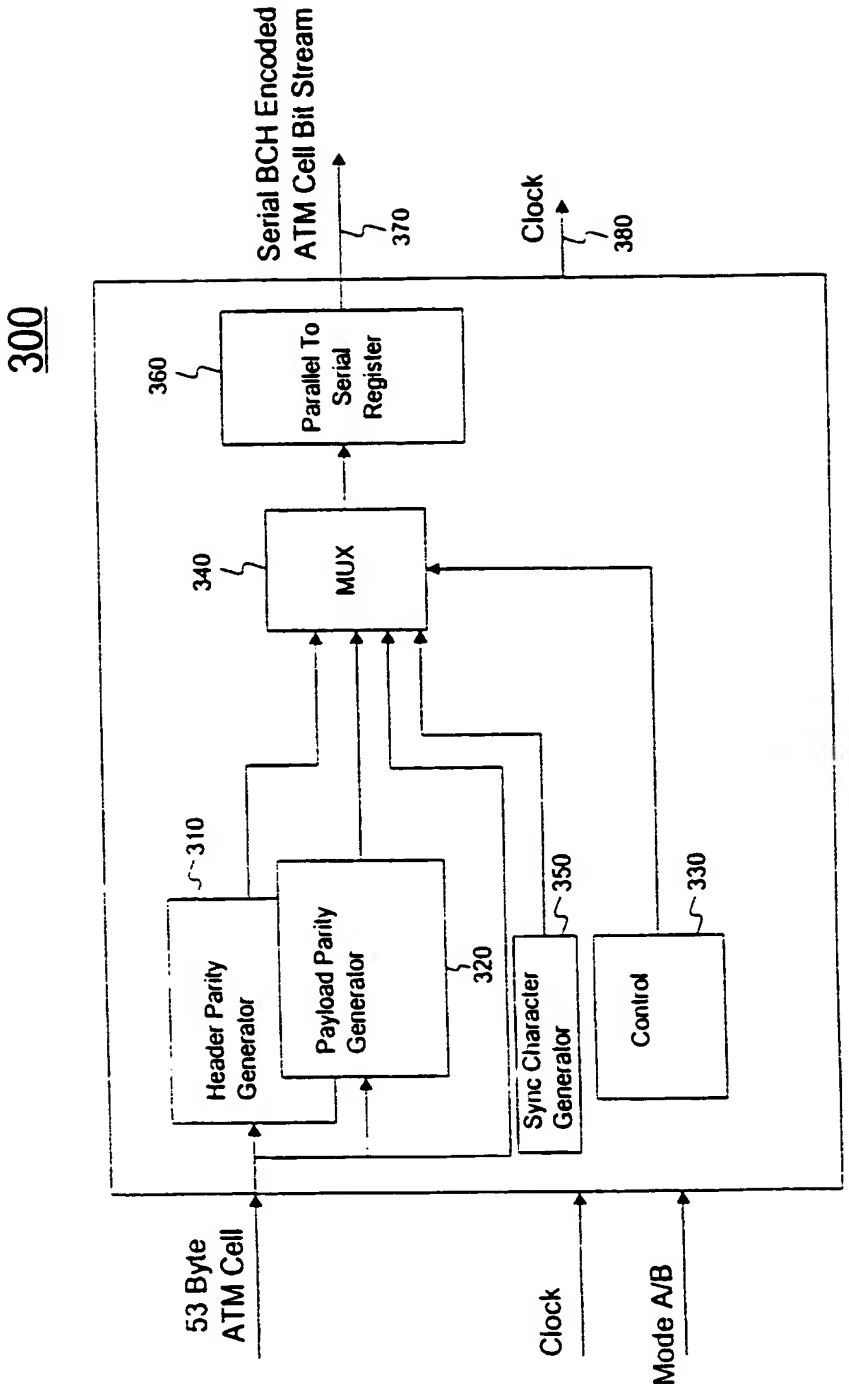

300
Serial BCH Encoded ATM Cell Bit Stream
370
Clock
380
360
Parallel To Serial Register
340
MUX
310
Header Parity Generator
Payload Parity Generator
320
350
Sync Character Generator
330
Control
53 Byte ATM Cell
Clock
Mode A/B

Figure 3

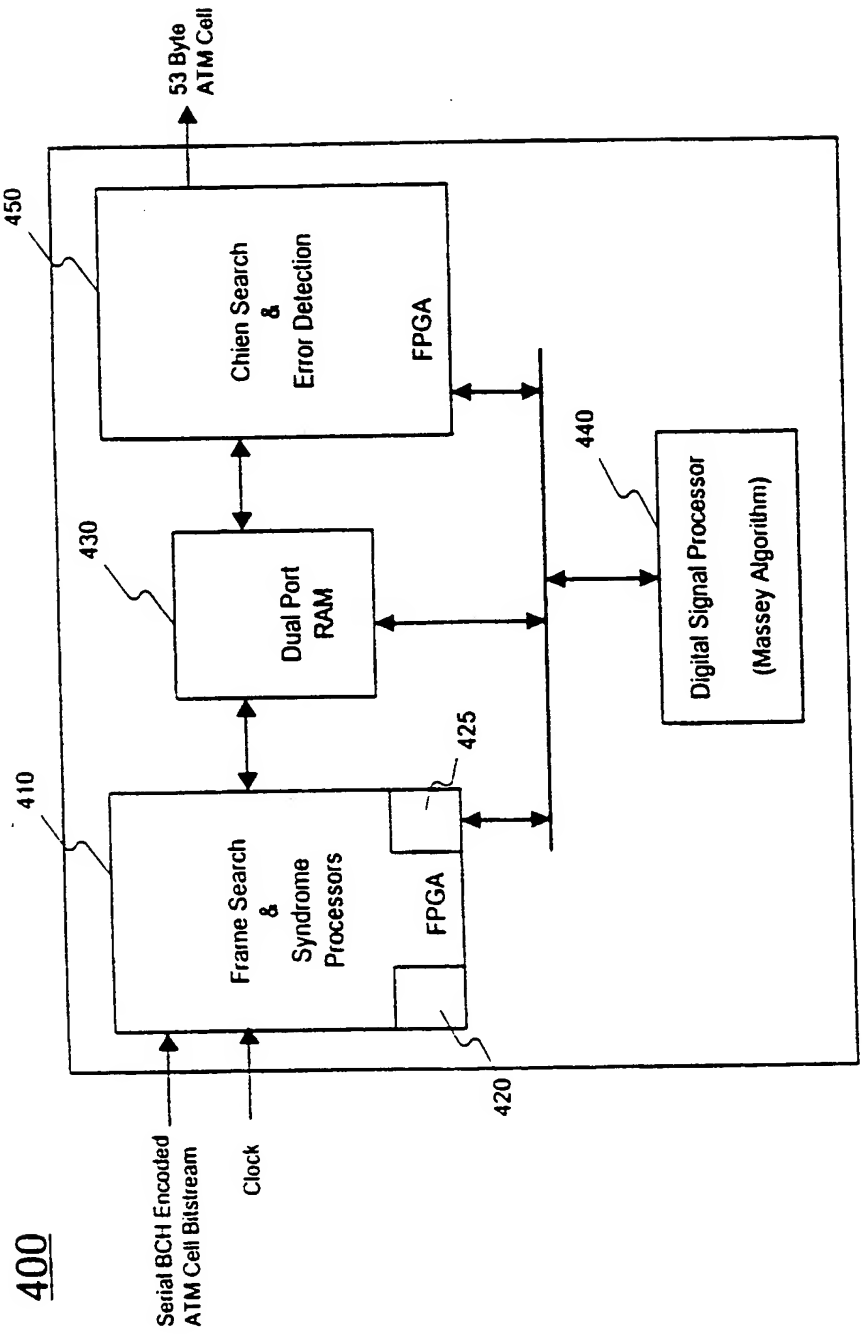

400
Serial BCH Encoded ATM Cell Bitstream
Clock
53 Byte ATM Cell
410
Frame Search & Syndrome Processors
FPGA
425
420
430
Dual Port RAM
440
Digital Signal Processor (Massey Algorithm)
450
Chien Search & Error Detection
FPGA

Figure 4

510

GENERALIZED SHIFT REGISTER MASK VALUES FOR FEEDBACK CONTROL (HEX)
USED BY SYNDROME AND CHIEN SEARCH COMPUTERS

NUMBER OF ERRORS CORRECTED : 1
PRIMATIVE POLYNOMIAL: 89(H)
GENERATOR POLYNOMIAL: 89(H)

	S1/C1	S2/C2	S3/C3	S4/C4	S5/C5	S6/S6	S7/C7	S8/C8	S9/C9	S10	S11	S12	S13	S14	S15	S16	S17	S18
m0	40	20	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
m1	01	40	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
m2	02	01	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
m3	44	22	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
m4	08	44	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
m5	10	08	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
m6	20	10	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00

511

GENERALIZED SHIFT REGISTER MASK VALUES FOR FEEDBACK CONTROL (HEX)
USED BY SYNDROME AND CHIEN SEARCH COMPUTERS

NUMBER OF ERRORS CORRECTED : 2
PRIMATIVE POLYNOMIAL: 89(H)
GENERATOR POLYNOMIAL: 4377(H)

	S1/C1	S2/C2	S3/C3	S4/C4	S5/C5	S6/S6	S7/C7	S8/C8	S9/C9	S10	S11	S12	S13	S14	S15	S16	S17	S18
m0	40	20	10	08	00	00	00	00	00	00	00	00	00	00	00	00	00	00
m1	01	40	20	10	00	00	00	00	00	00	00	00	00	00	00	00	00	00
m2	02	01	40	20	00	00	00	00	00	00	00	00	00	00	00	00	00	00
m3	44	22	11	48	00	00	00	00	00	00	00	00	00	00	00	00	00	00
m4	08	44	22	11	00	00	00	00	00	00	00	00	00	00	00	00	00	00
m5	10	08	44	22	00	00	00	00	00	00	00	00	00	00	00	00	00	00
m6	20	10	08	44	00	00	00	00	00	00	00	00	00	00	00	00	00	00

512

GENERALIZED SHIFT REGISTER MASK VALUES FOR FEEDBACK CONTROL (HEX)
USED BY SYNDROME AND CHIEN SEARCH COMPUTERS

NUMBER OF ERRORS CORRECTED : 3
PRIMATIVE POLYNOMIAL: 89(H)
GENERATOR POLYNOMIAL: 26D9E3(H)

	S1/C1	S2/C2	S3/C3	S4/C4	S5/C5	S6/S6	S7/C7	S8/C8	S9/C9	S10	S11	S12	S13	S14	S15	S16	S17	S18
m0	40	20	10	08	44	22	00	00	00	00	00	00	00	00	00	00	00	00
m1	01	40	20	10	08	44	00	00	00	00	00	00	00	00	00	00	00	00
m2	02	01	40	20	10	08	00	00	00	00	00	00	00	00	00	00	00	00
m3	44	22	11	48	64	32	00	00	00	00	00	00	00	00	00	00	00	00
m4	08	44	22	11	48	64	00	00	00	00	00	00	00	00	00	00	00	00
m5	10	08	44	22	11	48	00	00	00	00	00	00	00	00	00	00	00	00
m6	20	10	08	44	22	11	00	00	00	00	00	00	00	00	00	00	00	00

FIGURE 5A

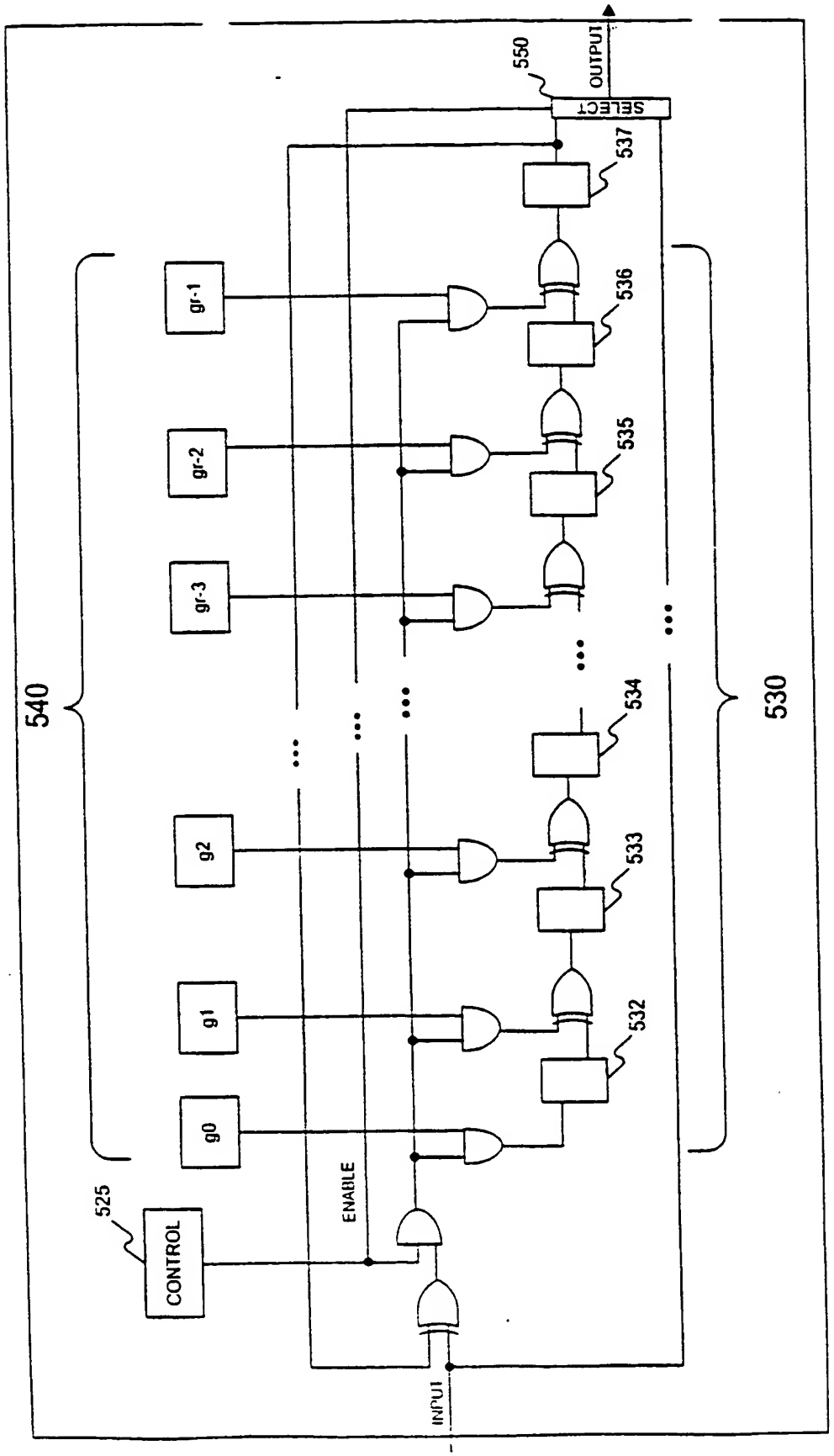

520
540
530
550
OUTPUT
SELECT
537
536
535
534
533
532
gr-1
gr-2
gr-3
g2
g1
g0
525
CONTROL
ENABLE
INPUT

Figure 5B

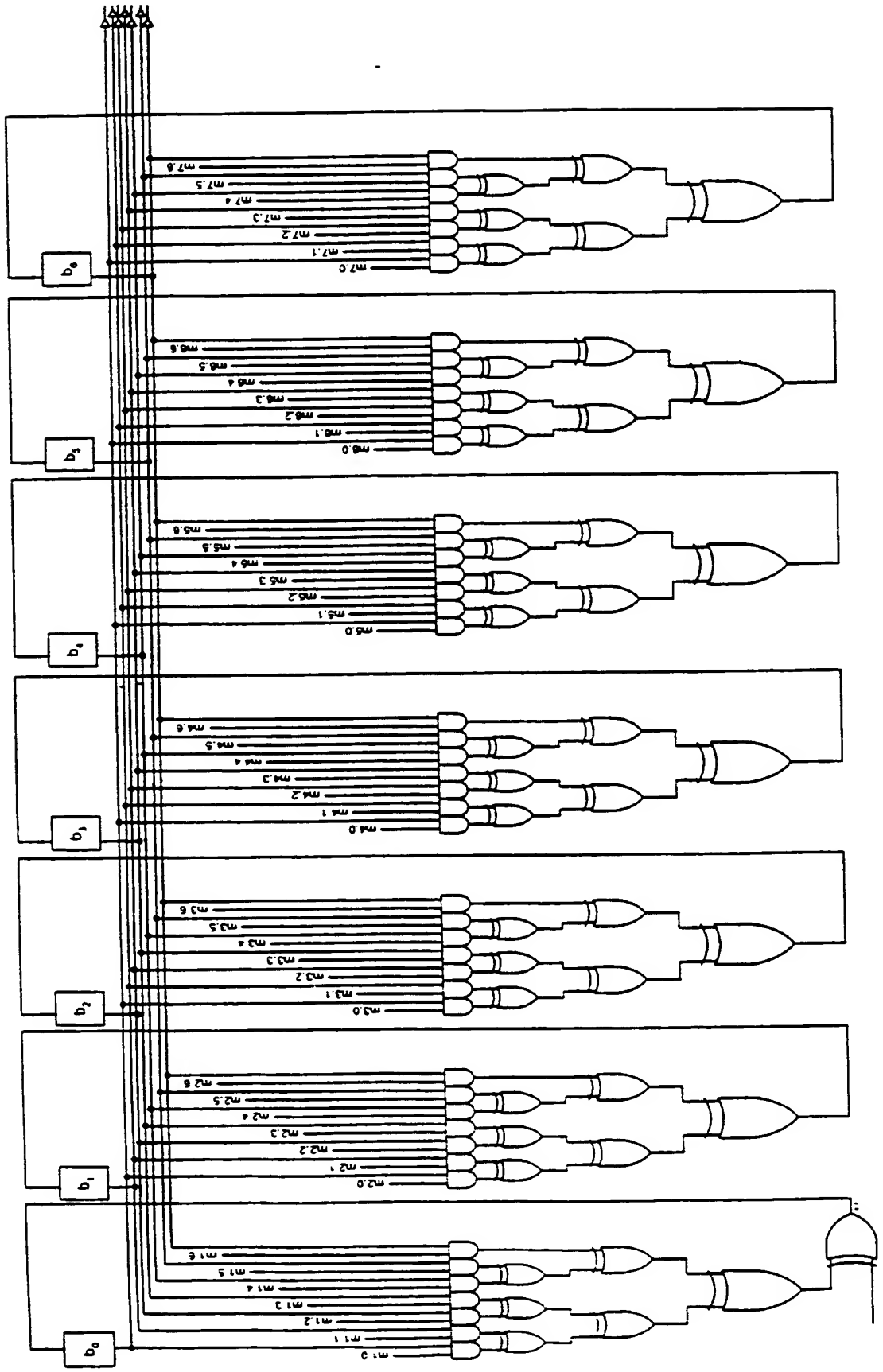


FIGURE 5C

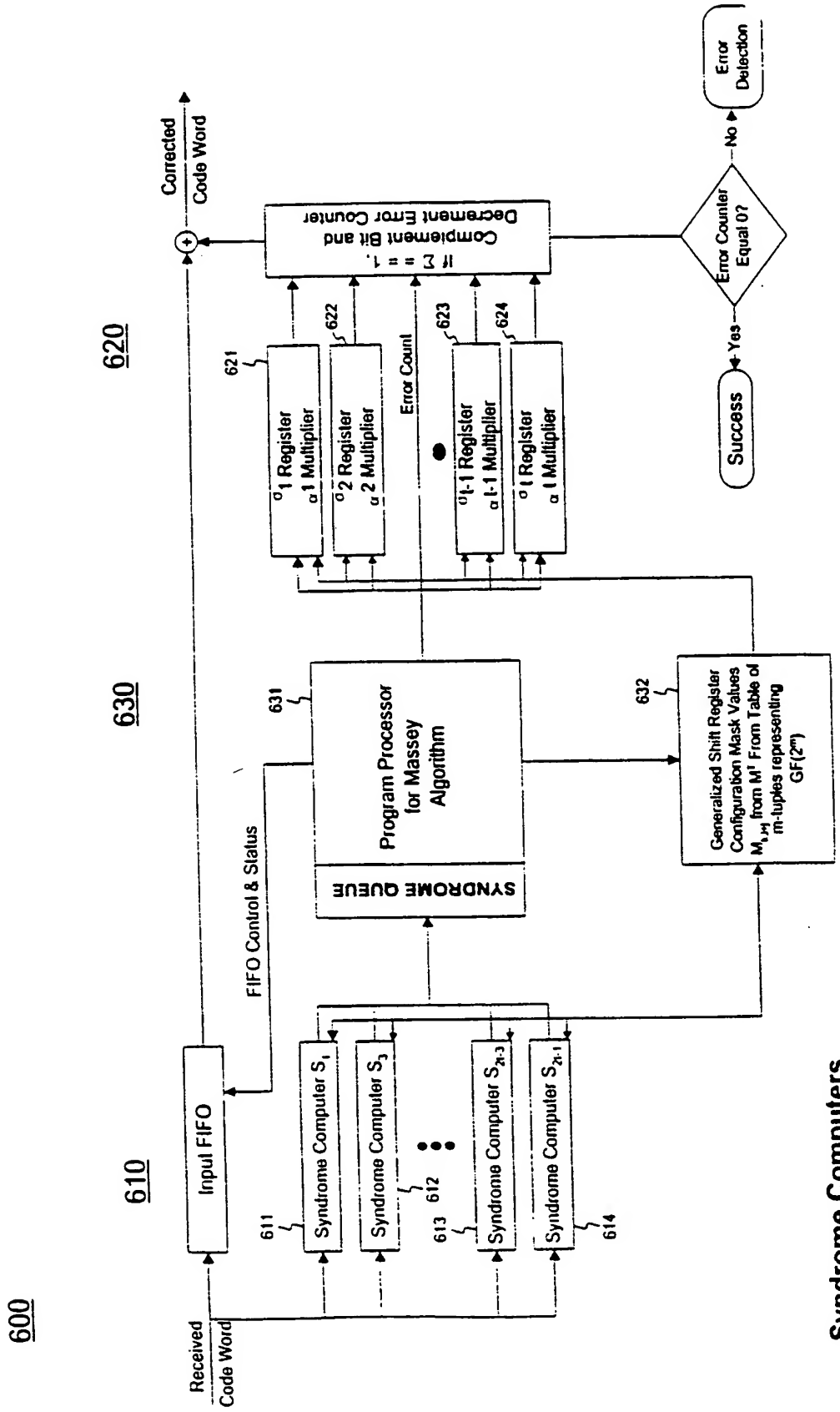

600
610
620
630
Received Code Word
Input FIFO
FIFO Control & Status
Syndrome Computer S_1
Syndrome Computer S_3
Syndrome Computer S_{2t-3}
Syndrome Computer S_{2t-1}
611
612
613
614
Syndrome Computers
SYNDROME QUEUE
631
Program Processor for Massey Algorithm
632
Generalized Shift Register Configuration Mask Values $M_{s,H}$ from M^1 From Table of m-tuples representing GF(2^m)
Massey Processor
621
622
623
624
σ_1 Register α 1 Multiplier
σ_2 Register α 2 Multiplier
σ_{t-1} Register α t-1 Multiplier
σ_t Register α t Multiplier
Error Count
Complement Bit and Decrement Error Counter
Chien Search
Error Counter Equal 0?
No
Yes
Success
Error Detection
Corrected Code Word

Figure 6

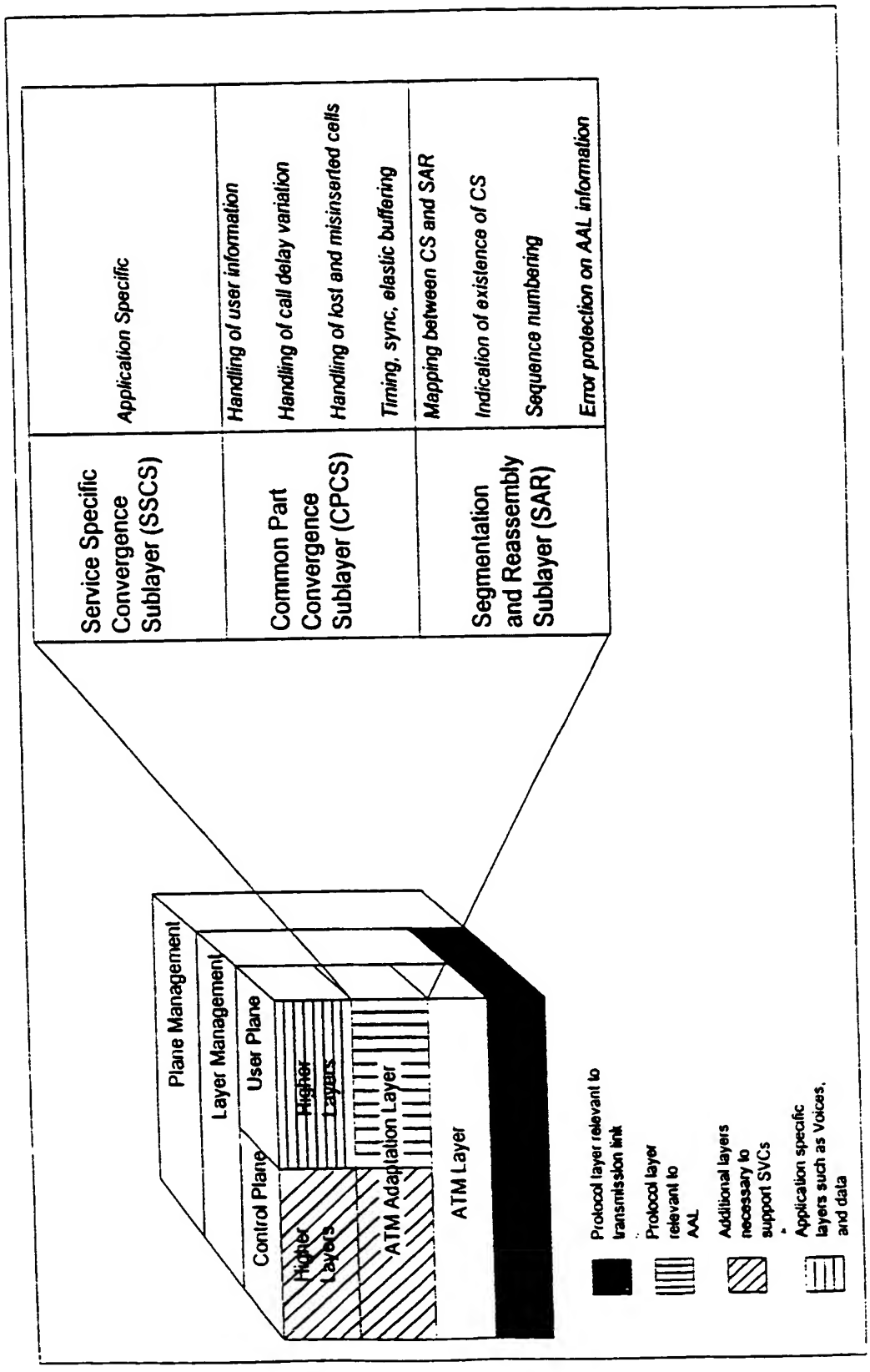

Service Specific Convergence Sublayer (SSCS)
Application Specific
Common Part Convergence Sublayer (CPCS)
Handling of user information
Handling of call delay variation
Handling of lost and misinserted cells
Timing, sync, elastic buffering
Segmentation and Reassembly Sublayer (SAR)
Mapping between CS and SAR
Indication of existence of CS
Sequence numbering
Error protection on AAL information
Plane Management
Layer Management
User Plane
Control Plane
Higher Layers
Higher Layers
ATM Adaptation Layer
ATM Layer
Protocol layer relevant to transmission link
Protocol layer relevant to AAL
Additional layers necessary to support SVCs
Application specific layers such as Voices, and data

Figure 7

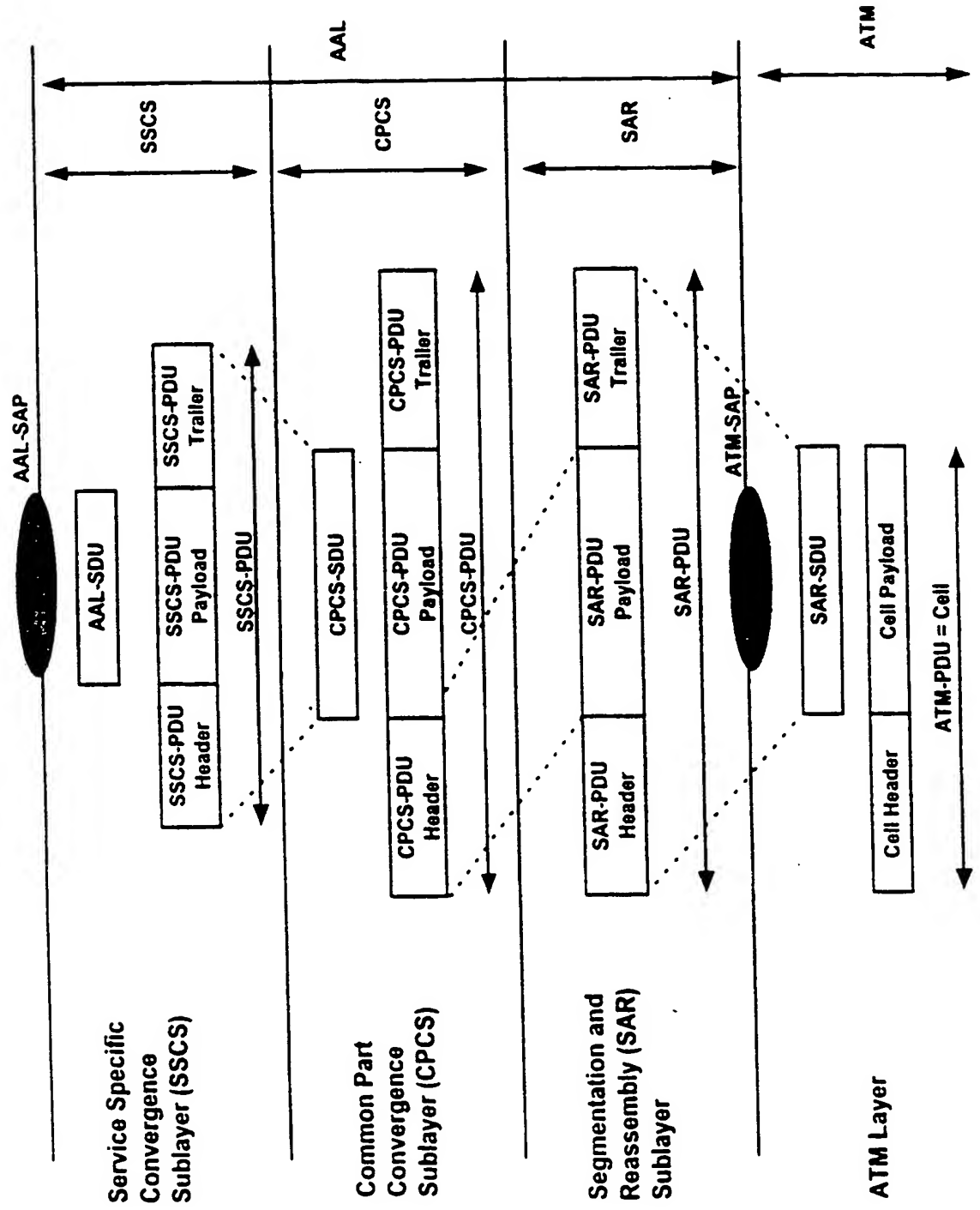

AAL
ATM
SSCS
CPCS
SAR
AAL-SAP
ATM-SAP
AAL-SDU
SSCS-PDU Header
SSCS-PDU Payload
SSCS-PDU Trailer
SSCS-PDU
CPCS-SDU
CPCS-PDU Header
CPCS-PDU Payload
CPCS-PDU Trailer
CPCS-PDU
SAR-PDU Header
SAR-PDU Payload
SAR-PDU Trailer
SAR-PDU
SAR-SDU
Cell Header
Cell Payload
ATM-PDU = Cell
Service Specific Convergence Sublayer (SSCS)
Common Part Convergence Sublayer (CPCS)
Segmentation and Reassembly (SAR) Sublayer
ATM Layer

Figure 8

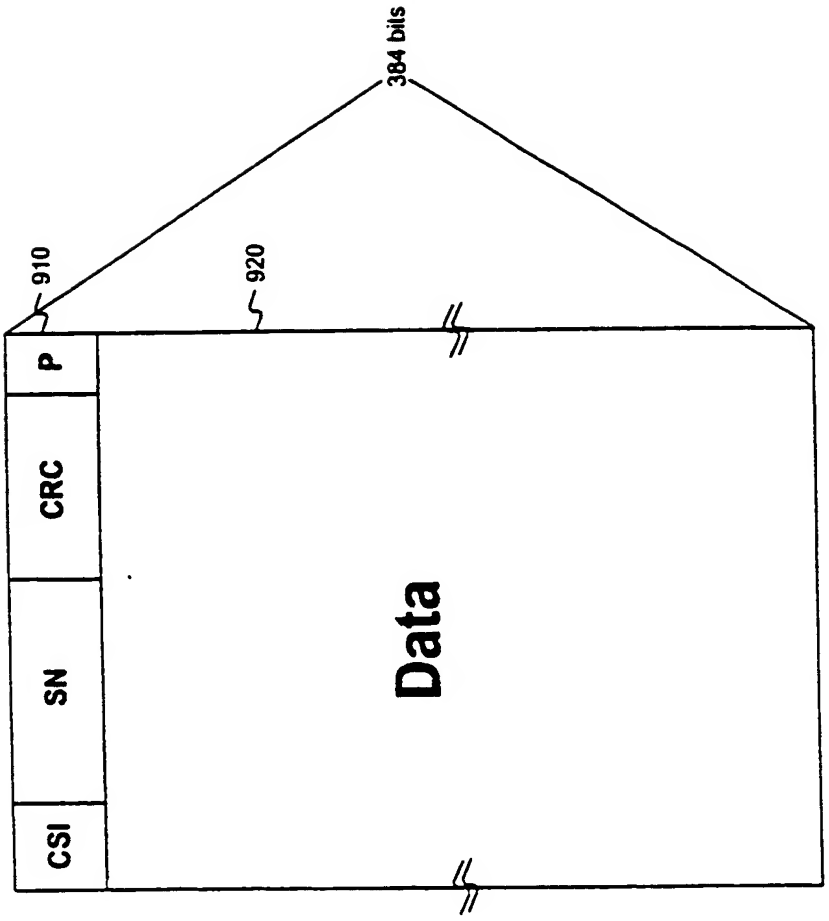


Figure 9

INTERNATIONAL SEARCH REPORT

Internati Application No
PCT/US 93/01926

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H04Q11/04

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H04Q H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No
X A	EP 0 713 347 A (AT & T CORP) 22 May 1996 see column 6, line 28 - line 35	1-5,25 13-24, 37-54, 133,138, 147
Y	see column 15, line 56 - column 16, line 45; figure 5 see figure 8 --- -/--	9-12, 33-36

[X] Further documents are listed in the continuation of box C

[X] Patent family members are listed in annex.

* Special categories of cited documents

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
10 September 1998	12. 10. 98

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Gregori, S

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Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Internati. Application No
PCT/US 98/01926

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No
X	RAYCHAUDHURI D: "WIRELESS ATM: AN ENABLING TECHNOLOGY FOR MULTIMEDIA PERSONAL COMMUNICATION" WIRELESS NETWORKS, vol. 2, no. 3, August 1996, pages 163-170, XP000625336 * sections 2.5, 2.6 * see figures 2,6,7 ---	151,156, 161,166
A	MILLER G J ET AL: "RELIABLE END-TO-END COMMUNICATION IN THE TACTICAL ATM ENVIRONMENT" MILCOM 1996. PROCEEDINGS OF THE 15TH. ANNUAL MILITARY COMMUNICATION CONFERENCE, MCLEAN, VA., OCT. 21 - 24, 1996, vol. VOL. 1, no. CONF. 15, 22 October 1996, pages 144-150, XP000697264 INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS * section 4.1 * see figure 4.1 ---	1-8, 25-32, 36, 133-170
A	FARSEROTU J ET AL: "TCP/IP OVER LOW RATE ATM-SATCOM LINKS" MILCOM 1996. PROCEEDINGS OF THE 15TH. ANNUAL MILITARY COMMUNICATION CONFERENCE, MCLEAN, VA., OCT. 21 - 24, 1996, vol. VOL. 1, no. CONF. 15, 22 October 1996, pages 162-167, XP000697267 INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS * section 1 * see figure 2 ---	1-8, 25-32, 36, 133-170
X	AIKAWA S ET AL: "1996 IEEE INTERNATIONAL CONFERENCE ON COMMUNICATIONS (ICC), CONVERGING TECHNOLOGIES FOR TOMORROW'S APPLICATIONS DALLAS, JUNE 23 - 27, 1996" 1996 IEEE INTERNATIONAL CONFERENCE ON COMMUNICATIONS (ICC), CONVERGING TECHNOLOGIES FOR TOMORROW'S APPLICATIONS DALLAS, JUNE 23 - 27, 1996, vol. 1, 23 June 1996, pages 454-458, XP000625714 INSTITUTE OF ELECTRICAL & ELECTRONICS ENGINEERS	55-68
Y	* sections 3.1, 3.2, 3.3, 3.4 * see figures 2,3 --- -/--	9-12, 33-36

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INTERNATIONAL SEARCH REPORT

Internatic Application No
PCT/US 98/01926

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication where appropriate, of the relevant passages	Relevant to claim No.
X	TORRES P ET AL: "ADAPTIVE ERROR CONTROL CODING FOR A MOBILE BROADBAND SYSTEM" 1996 IEEE 46TH. VEHICULAR TECHNOLOGY CONFERENCE, MOBILE TECHNOLOGY FOR THE HUMAN RACE ATLANTA, APR. 28 - MAY 1, 1996, vol. 3, no. CONF. 46, 28 April 1996, pages 1751-1755, XP000595814 INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS * section III.B *	69,70, 72-74, 81,82, 84-86, 171-173, 181-183
X	EP 0 721 267 A (TOKYO SHIBAURA ELECTRIC CO) 10 July 1996	93,94, 102,191, 194
Y	see page 38, line 23 - page 42, line 56 see page 49, line 10 - line 11	96,97, 106,107
Y	EP 0 748 124 A (DISCOVISION ASS) 11 December 1996 see page 26, line 34 - line 49	96,97, 106,107
X	CA 2 159 440 A (COMSAT CORP) 31 March 1996 see page 4, line 10 - line 15 see page 6, line 19 - page 10, line 13	114,123
A	PIPER T T ET AL: "ATM-providing broadband services to the warrior" PROCEEDINGS OF THE 1994 TACTICAL COMMUNICATIONS CONFERENCE. VOLUME ONE. DIGITAL TECHNOLOGY FOR THE TACTICAL COMMUNICATOR (CAT. NO.94TH0678-3), PROCEEDINGS OF TCC'94 - TACTICAL COMMUNICATIONS CONFERENCE, FORT WAYNE, IN, USA, 10-12 MAY 1994, pages 217-224, XP002076940 ISBN 0-7803-2004-2, 1994, New York, NY, USA, IEEE, USA see page 224, column 1, line 10 - line 29	1-196

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INTERNATIONAL SEARCH REPORT

Intern. ...nal application No
PCT/US 98/01926

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This International Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons.

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the International Application that do not comply with the prescribed requirements to such an extent that no meaningful International Search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. [X] As all required additional search fees were timely paid by the applicant, this International Search Report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this International Search Report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this International Search Report is restricted to the invention first mentioned in the claims, it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

[X] No protest accompanied the payment of additional search fees

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. Claims: 1-8 , 25-32, 36 , 133-170

   Method and apparatus for creating a frame appending a different synchronization character to the cell on alternate frames

2. Claims: 1,4,9-12, 25,33-35, 55-68

   Method and apparatus for encoding the header portion of the cell separately from the payload portion using different error decting/correcting codes

3. Claims: 13-24, 37-54

   Method and apparatus for creating a frame placing into a header portion of the frame the header data from an ATM cell other than the error detecting/correcting codes

4. Claims: 69-92, 171-190

   Method and apparatus for selecting a code to match transmission characteristics of the channel

5. Claims: 93-113, 191-196

   Method and apparatus for computing syndromes of a received word and finding an error locator polynomial from the syndromes

6. Claims: 114-132

   Method and apparatus for transmitting a frame interleaving the payload bits and the header bits

INTERNATIONAL SEARCH REPORT

Information on patent family members

Internatic Application No
PCT/US 98/01926

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0713347 A	22-05-1996	US 5570355 A	29-10-1996
		CA 2162611 A	18-05-1996
		CN 1151094 A	04-06-1997
		JP 8251237 A	27-09-1996
EP 0721267 A	10-07-1996	JP 8186570 A	16-07-1996
EP 0748124 A	11-12-1996	CA 2170469 A	08-12-1996
		CN 1138795 A	25-12-1996
		JP 9008853 A	10-01-1997
		JP 10135941 A	22-05-1998
		JP 10093438 A	10-04-1998
		US 5717715 A	10-02-1998
		US 5635864 A	03-06-1997
		US 5668831 A	16-09-1997
		US 5692020 A	25-11-1997
		US 5761210 A	02-06-1998
CA 2159440 A	31-03-1996	US 5600653 A	04-02-1997